Low Power High Speed Square Root BK Carry Select Adder using MT CMOS Technique in Cadence Tool

P. Chandra Sekhar –CBIT-Hyderabad

Abstract- Adder is a digital circuit that performs addition of numbers. Ripple Carry Adder (RCA) shows the compact design but their propagation delay is more. Propagation delay of Carry Look-Ahead Adder (CLA) is small but it consumes more area and power. To compromise propagation delay and area problems Carry Select Adder (CSA) is used. To perform fast arithmetic operations at smaller area consumption, Carry Select Adder (CSA) is one of the fastest adders used in many data- processing processors. The structure of CSA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate level change is used to reduce the area, delay and power of CSA.

Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. Regular Square Root BK (SRBK) CSA and Modified SRBK CSA are designed. Regular SRBK CSA is designed by replacing one row of RCA with BK adder and Modified SRBK Adder is designed by further replacing second row of RCA in SRBK Adder with Binary to Excess-1 (BEC). For further reducing power consumption and delay, all the circuits are implemented using MTCMOS technique. MTCMOS technique is an effective solution for high-speed low-power applications. Power and delay of all these adders are calculated at different input voltages. The results depict that Modified SQRT BK CSA is better than all the other adder architectures in terms of power but with small speed penalty. With respect to delay SQRT BK CSA is better than all the other adder architectures. The designs have been synthesized at 180nm technology using Cadence tool.

Keywords- Full Adder, Ripple Carry Adder, BK Adder, SRBK Adder, Modified SRBK Adder, MTCMOS.

I. INTRODUCTION

In any electronic devices, adders are not only used in the arithmetic logic unit (ALU), but also used in other processing units, where they are used to calculate addresses, table indices and similar applications. Some other applications of adders are in digital signal processor (DSP) as a Multiply-Accumulation unit (MAC), and also used in multipliers, high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR.

The different Adder topologies such as Ripple Carry Adder (RCA), Carry look-Ahead Adder (CLA) and Carry Select Adder (CSA). Based on area, delay and power consumption one of the adder is used. Ripple Carry Adder (RCA) have the compact design but their propagation delay is more. Carry Look-Ahead Adder (CLA) is used to derive fast results but it leads to increase in area. Longer propagation delay and more area consumptions are the two disadvantages. These disadvantages are overcome by using Carry Select Adder (CSA). Carry Select Adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder.

This paper presents a comparative analysis of various adders and proposed design of SRBK CSA by using BK Adder and Ripple Carry Adder and modified SRBK CSA using BK Adder and Binary to Excess-1 Converter (BEC). Both these adders implemented using MTCMOS technique and shows less area, delay and power than other adders.

II. LITERATURE SURVEY

Ripple Carry Adder consists of cascaded of "N" single bit full adders. Output carry of one adder becomes the input carry of other full adder and so on. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Figure 1 shows the schematic block diagram of four bit ripple carry adder. As the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. Now CSA provides a way to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. Therefore the conventional CSA makes use of Dual RCA's to generate the partial sum and carry by considering input carry Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers which is shown in figure 2. The conventional CSA is area consuming due to the use of dual RCA's.

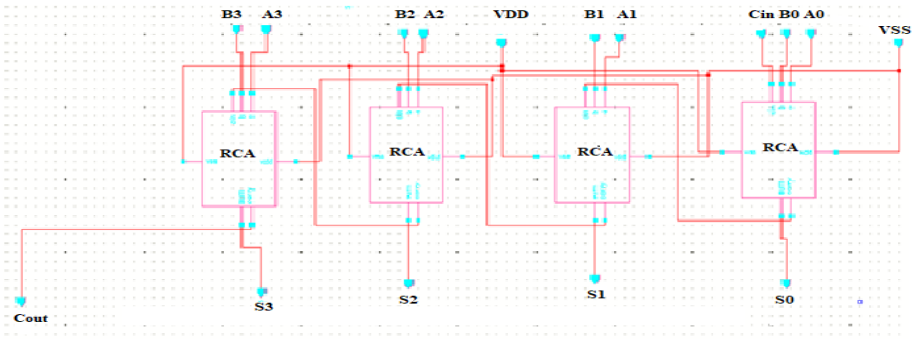

Fig.1: 4-bit Ripple Carry Adder

The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with Cin=1 in conventional CSLA in order to reduce the area and power. BEC uses less number of logic gates than N-bit full adder structure. To replace N-bit RCA, an N+1 bit BEC is required. Therefore, Modified CSLA has low power and less area than conventional CSLA. SQRT CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and low power. Regular SQRT CLA also uses dual RCAs. In order to reduce the delay, area and power, the design is modified by using BEC instead of RCA with Cin=1. Therefore, the modified SQRT CLA occupies less area, delay and low power. Further also, the parameters like delay, area and power can be reduced.

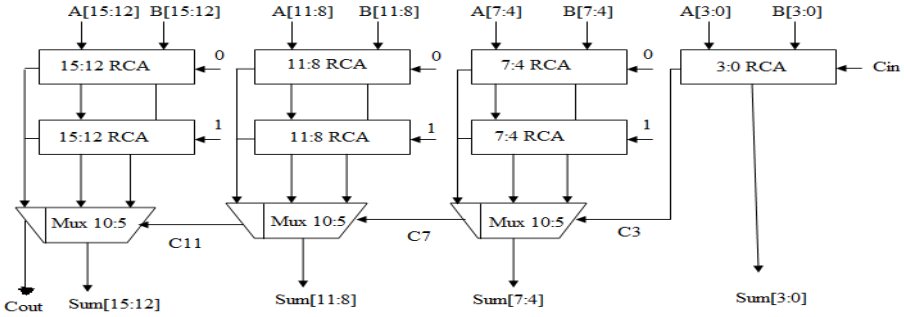

Fig.2: 16-bit conventional carry select adder

III. BK ADDER

Brent-Kung adder is a one of the parallel prefix adder which gives higher regularity to the adder structure and has less wiring congestion leading to better performance and less necessary chip area. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in Brent Kung adders. The block diagram of 4-bit Brent-Kung adder is shown in Figure.3.

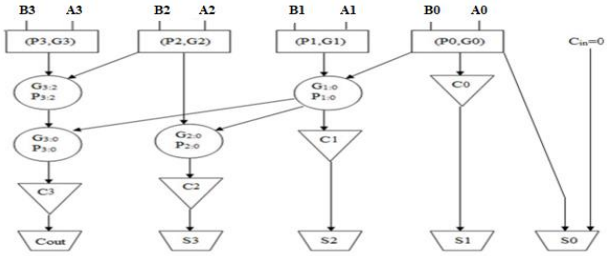

Fig.3: Block Diagram of 4-Bit Brent Kung Adder

Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation. The construction of parallel prefix adder involves three stages:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

Pre- processing stage:

Generate and propagate signals to each pair of inputs A and B are computed in this stage as shown in figure 3. These signals are given by the following equations 1 & 2:

$$P_i = A_i \oplus B_i \quad 1$$

$$G_i = A_i \cdot B_i \quad 2$$

Carry generation network

In this stage, we compute carries equivalent to each bit. Implementation of these operations is carried out in parallel.

After the computation of carries in parallel they are segmented into smaller pieces. Carry propagate and generate are used as intermediate signals which are given by the logic.

$$CP_{i:j} = P_{i:k+1} \square P_{k:j} \quad 3$$

$$CG_{i:j} = G_{i:k+1} + (P_{i:k+1} \square G_{k:j}) \quad 4$$

This is the concluding step to compute the summation of input bits. It is common for all the adders and the sum bits are computed by logic equation 5 & 6:

$$C_{i-1} = (P_i \,.\, C_{in}) + Gi \quad 5$$

$$S_i = P_i \oplus C_{i-1} \quad 6$$

Post processing stage

IV. Regular Square Root BK Carry Select Adder

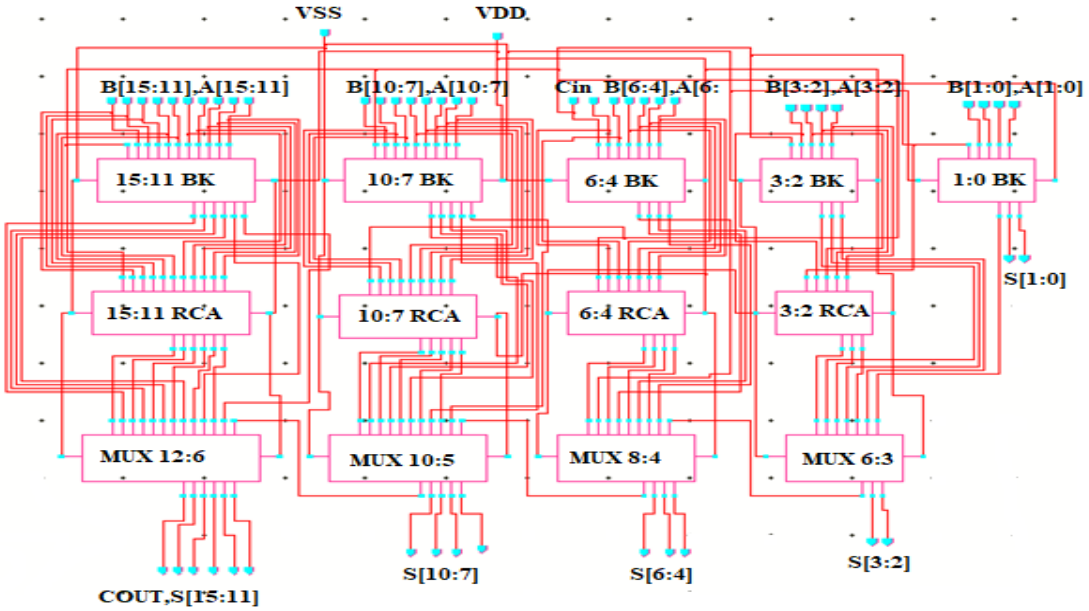

Fig.4: The schcmatic diagram of 16-bit Regular SRBK CSA

The schematic of 16-bit Regular Square Root BK Carry Select Adder is shown in Fig. 4. There are 5 groups in Regular Square Root BK Carry Select Adder. Here single Brent Kung adder is used for Cin=0 and ripple carry adder is used for Cin=l and then there is a multiplexer stage. Due to the presence of RCA and BK, this circuit consumes large area.

V. MODIFIED SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Binary to Excess- 1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified in order to obtain a reduced area and power consumption. Binary to Excess-l converter is used to add 1 to the input numbers. So, here Brent Kung adder with Cin=1 will be replaced by BEC because it require less number of logic gates for its implementation so the area of circuit is less. A circuit of 4-bit BEC and truth table is shown in Fig.4 and Table 1 respectively.

Modified Square Root Brent Kung Carry Select Adder has been designed using Brent Kung adder for Cin=0 and BEC for Cin=l and then there is a multiplexer stage. It has 5 groups of different size brent kung adder and Binary to Excess-l Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA therefore it consumes less area.

Each group contains one BK, one BEC and MUX. For N Bit Brent Kung adder, N+1 Bit BEC is used. Fig. 6 shows the schematic of 16-Bit Modified SQRT CSA. Power consumption and delay of this adder is calculated for 8-bit and 16-Bit word size.

TABLE 1: Truth Table of 4-Bit Binary to Excess-1 Converter

Binary Logic B0 B1 B2 B3	**Excess-1 Logic X0 X1 X2 X3**
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101

0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

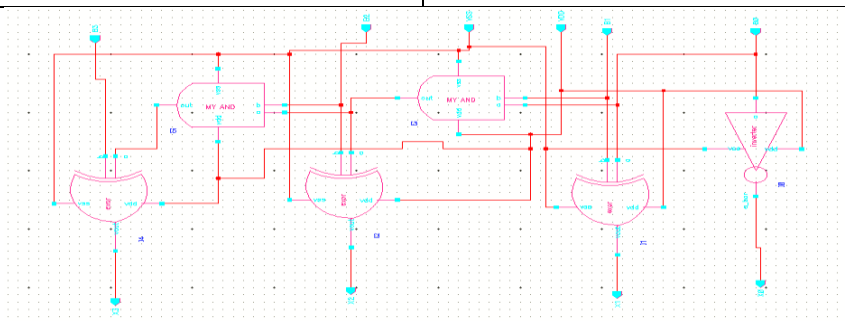

Fig.5: 4-bit Binary to Excess-I code Converter

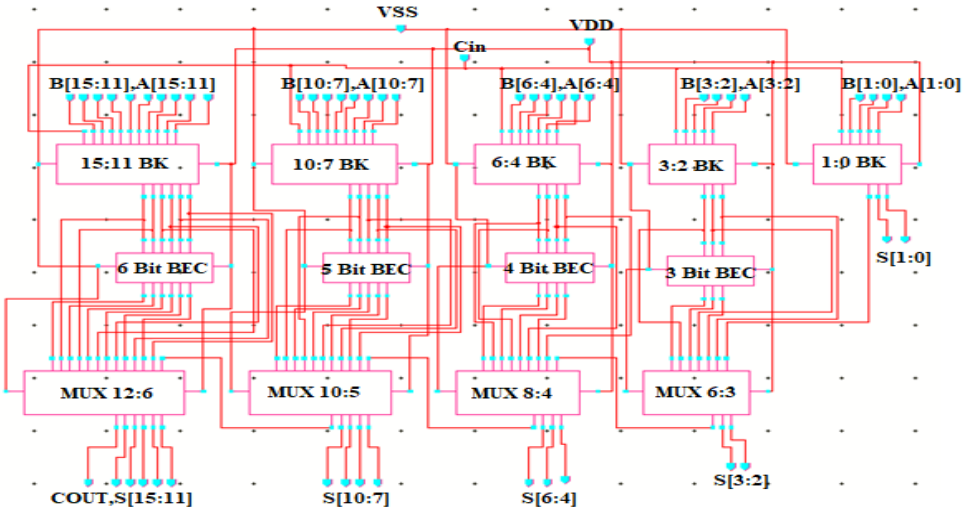

Fig.6: Schematic of 16-Bit Modified SQRT BK CSA

VI. SIMULATION RESULTS AND COMPARISON

Various adders were designed in CADENCE Virtuoso of version 5.6.1 tool using 180nm MTCMOS technology. Power consumption and delay of various adders like Conventional Dual Ripple Carry Adder, Regular SRBK CSA, Modified SRBK CSA with and without MTCMOS technique has been calculated for 16-Bit word size. The comparison of various adders for different parameters like delay and power consumption is shown in Table 2. The result analysis shows that Modified Square Root Brent Kung Carry Select Adder shows better results than all the other adder architectures in terms of power consumption but with a small speed penalty. Regular SRBK CSA with MTCMOS technique has less delay among all the adders and Modified SRBK with MTCMOS has highest delay. The power consumption is minimum in Modified SRBK with MTCMOS and maximum in Conventional Dual RCA without MTCMOS. As we know Energy is the product of power and delay. The Energy consumption is less in Regular SRBK with MTCMOS and it is highest in Dual RCA without MTCMOS as shown in Table 2 and graphical representation of all these comparisons of different adders are shown in Figure 7.

The power and Delay variation at different input voltages of 8-Bit and 16-Bit word size are depicted in Table 3 and Table 4 respectively.

Table 2 Comparison of power and delay of Different Adder topologies

Adder	Delay (in ps)	Power (in uW)	Power Delay Product(fWs)
Conventional (Dual RCA)	410	841.9	345.18
Dual RCA with MTCMOS	364.5	799.5	291.42
Regular SRBK without MTCMOS	331.9	776	257.56
Regular SRBK with MTCMOS	302	230.8	69.7
Modified SRBK without MTCMOS	383.6	669.5	256.82
Modified SRBK with MTCMOS	685.6	220.6	151.46

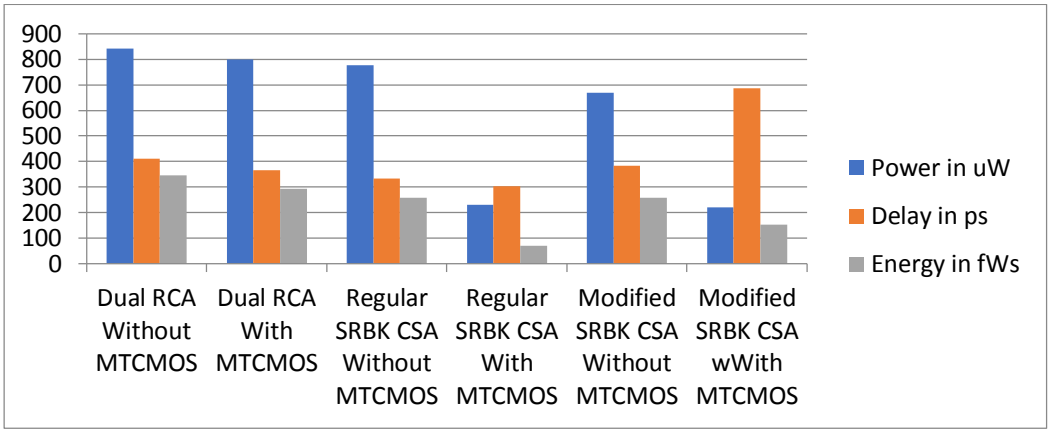

Fig.7: Graphical representations of Different Adder Topologies

The graphical representation of comparison of Regular SRBK CSA and Modified SRBK CSA of 8-Bit size at different input voltages for power consumption and delay is shown in figure 8. Results show that modified SRBK CSA shows better results than Regular SRBK CSA in terms of power consumption. The graphical representation of comparison of Regular SRBK CSA and Modified SRBK CSA of 16-Bit word size for power consumption and delay at different input voltages is shown in Figure 9.

Table 3 Comparison of SRBK and Modified SRBK adders of 8-bit at different input voltages

Input Voltage(in V)	SRBK ADDER 8-BIT		MODIFIED SRBK 8-BIT	
	POWER(in micro Watts)	DELAY(in ps)	POWER(in micro Watts)	DELAY(in ps)
1	774	233.2	514.2	648.7
1.2	311.6	297.9	228.3	720.2
1.4	173.7	304.5	139.4	733.8
1.6	168.5	323	135.4	657.2
1.8	168.3	337.5	135.6	657.7

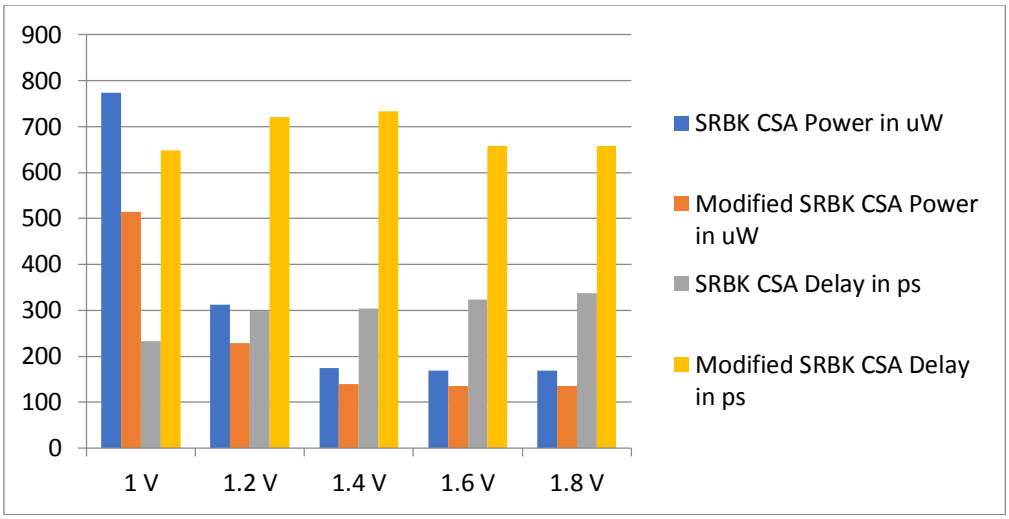

Fig.8: Comparison of Regular SQRT BK CSA and Modified SQRT BK CSA of 8-Bit for power and delay comparison at different input voltages

As the input voltage increases the power consumption decreases and the delay increases as shown in figure 8 and figure 9.

Table 4 Comparison of SRBK and Modified SRBK adders of 16-bit at different input voltages

Input Voltage(in V)	SRBK ADDER 16-BIT		MODIFIED SRBK 16-BIT	
	POWER(in micro Watts)	DELAY(in ps)	POWER(in micro Watts)	DELAY(in ps)
1	845.3	214.5	581	667.5
1.2	371.8	249.1	314.4	674.4
1.4	233.7	270.6	231.5	679.7
1.6	229.6	288.2	222.5	683.4
1.8	230.8	302	220.6	685.6

From the Table 3 and Table 4, it is concluded that the power consumption is very less in Modified SRBK CSA as compared with remaining adders. And Regular SRBK CSA is highest speed adder among all the adders.

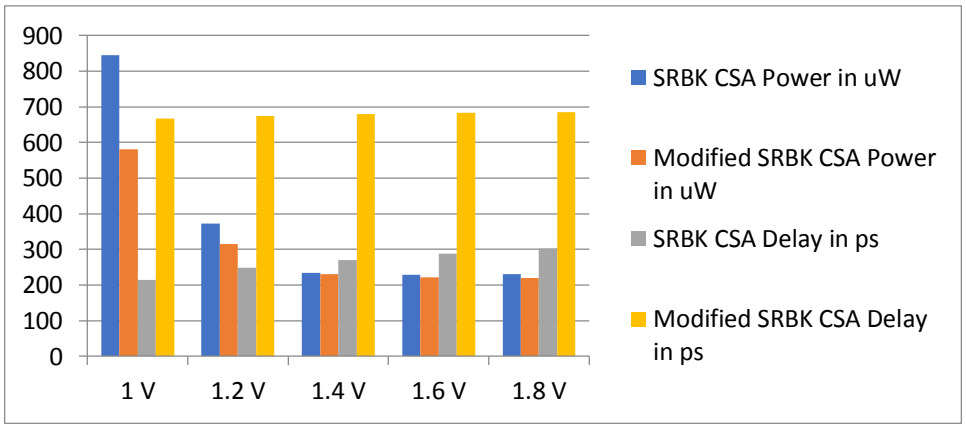

Fig.9: Comparison of Regular SQRT BK CSA and Modified SQRT BK CSA of 16-Bit for power and delay comparison at different input voltages

VII. CONCLUSION

Power, delay and area are the main factors in VLSI design that limits the performance of any circuit. This work presents a simple approach to reduce the area, delay and power of CSA architecture. The conventional carry select adder has the disadvantage of more power consumption and occupying more chip area. The proposed Modified SRBK CSA using MTCMOS technique has low power and reduced area at small speed penalty than all the other adder structures. The proposed Adder structures exhibits a higher speed and lower power consumption compared with those of the conventional adders. The speed enhancement have achieved by modifying the structure through by adding a Brent Kung Carry Select Adder which is much faster when compared to dual ripple carry adder. Square Root Brent Kung Carry Select Adder with MTCMOS has the less power consumption and lesser delay. So, these adders are best suited design for high speed low power applications.

VIII. FUTURE WORK

The work can be further extended by applying the Brent Kung Adder with MTCMOS technique in Booth Multiplier and various Multipliers. The use of Brent Kung Adder with MTCMOS technique helps in reducing power and delay in the circuit.

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