A Single Phase Newly Proposing 85 Level Asymmetric Multi-Cell Cascaded Multilevel Inverter with Reduced Number of Switches

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***Abstract*—In a short while ago, a various multilevel designs cameinto presence. From that designs cascaded multilevel inverter is mostly used structure. This type of multilevel inverter integrates a medium voltage output on the base of series connection of power cells in which it uses standard low voltage component configurations. This peculiar confess one to achieve high quality output voltage and current waveform by using different topologies. So the objective of this paper is to get higher output voltage level with less number of switches, less cost and lower THD values. It is achieved by asymmetric multi-cell CMLI topology. Hence this paper inaugurates a newly proposing 85 level asymmetric multi-cell cascade multilevel inverter. This is the best topology to improve the fundamental component and also to reduce the THD value by using the less number of switches while comparing to other topologies of CMLI. In order to verify the newly proposed topology MATLAB/SIMULINK software is used and the results will be present.**

Keywords: cascaded multi-level inverter (CMLI), multi-cell, total harmonic distortion (THD).

I. INTRODUCTION

Inverter is an electrical power converter which changes fixed DC voltage to variable AC voltage. The inverter doesn't produce a pure sinusoidal wave form because an infinite number of odd harmonics present in it. If the square wave is used for the electrical equipment's it decreases the life span of electrical equipment's. This disadvantage is rectified by using multilevel inverters in which produces staircase voltage wave form which is equal to sinusoidal wave form [1], [2].

Multilevel inverters are referring to the various voltage values in a cycle. It is adorable solution for medium voltage and high power applications. The basic consideration of a multilevel inverter is to use a series of power semiconductor switches in order to combine a staircase voltage waveform with peak value which is equals to the entity of the multiple input DC sources. The input sources can be taken as batteries, PV cells, fuel cells etc. The power semiconductor switches are supervised to sum of these multiple DC sources to acquire high output voltage. The most common semiconductor switching devices are MOSFET, IGBT. A typical power inverter circuits or devices require a relatively stable DC power source capable of supplying enough current for the intended power demands of the system. The input voltage depends on the design and power of the inverter.

Multilevel inverters are of three types which are namely as Diode clamped, Flying capacitor and cascaded H-Bridge multilevel inverters. Among all topologies, CMLI attains the higher output voltage and power levels and higher reliability due to its standard topology. Again CMLI can be classified into two types which are symmetrical and asymmetrical cascaded multilevel inverters [3], [4]. Among that symmetrical CMLI means the input DC sources of the CMLI are equal in magnitude. Whereas Asymmetric CMLI means the input DC sources are not equal in magnitude. By comparing two multilevel inverters asymmetric CMLI requires least number of components to attain same number of voltage level. In this present paper, existing system of seven level inverter by using sinusoidal PWM technique and proposed system of 25 level Asymmetric multi-cell CMLI and newly proposed system of 85 level Asymmetric multi-cell CMLI are presented and also THD values are compared. And also LC filter are used then THD values are measured.

II. EXISTING SYSTEM

The existing system of this paper is to implement the seven level inverter using sinusoidal pulse width modulation technique. This technique is simple for harmonic reduction. In this technique the reference signal (sine wave) is compared to carrier signal which is triangular wave. Gate pulses are generated by comparing the two signals and sine wave has fundamental frequency in which carrier wave can be taken more than fundamental frequency ($f_c = M.I*f_r$).

Sinusoidal pulse with modulation is one of the ancient techniques which are used to decrease the harmonics presented in the quasi-square wave. In this modulation technique, there are two important defined parameters. They are 1. Modulation index frequency and 2. modulation index amplitude. Modulation index frequency means the ratio of reference frequency to the carrier frequency. And the ratio between reference signal amplitude and carrier signal amplitude is known as modulation index amplitude. For the seven levels inverter the phase shift will be 360/n-1 where n is number of levels i.e.., 7 hence the phase shift will be 60 degrees. The seven level inverter by using PWM technique circuit diagram as shown in Fig.1.

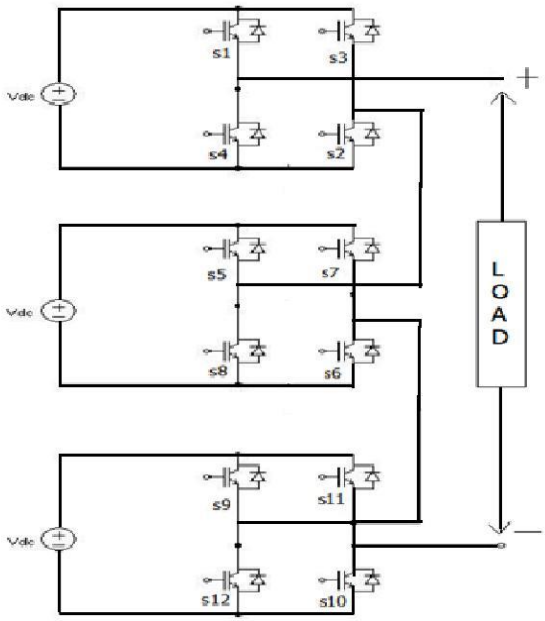

Fig. 1 Seven level inverter block diagram

In sinusoidal PWM technique, three full bridges are used. DC voltage sources of 100V, 100V, 100V is taken as inputs of three bridges. To turn on the switches gate pulse are required. For seven level the phase delays are 0, 60, 120, 180, 240, 300 degrees. Here the values used are L= 20mH, C=1µF.The output waveform and FFT Analysis are shown in simulation results.

III. PROPOSED SYSTEM

In this proposed system, 25 level multi-cell cascaded Multilevel inverter is presented. In this topology, high quality output voltage and current waveforms are obtained with less number of switching components. For example, to get 25 levels in this topology only 12 switches are required. In this multi-cell topology, multiple numbers of non-isolated DC voltage sources are given to the input. Other than the full bridge (4 switches) extra switching components are given to power cells as series and parallel connection. The first terminal taken from the first extremity of the first bridge is considered as the positive load terminal. The second extremity of first bridge is connected to first extremity of the second bridge circuit. This is nothing but cascaded connection of bridges. By this topology, switching losses are reduced, cost is effective, lower voltage rating devices can be used, leading to reduction in Electro Magnetic Interference and voltage stress (dv/dt) is decreased. Mainly this topology is used for low voltage high power applications like industries etc., 25 level asymmetric multi-cell CMLI block diagram is as shown in the Fig.2.

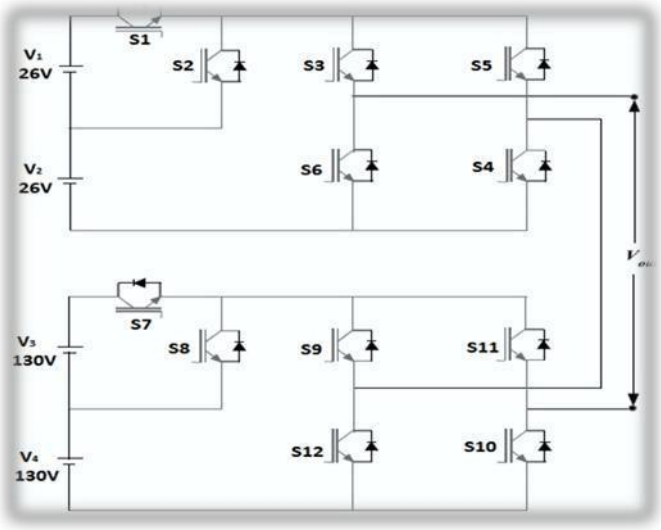

Fig. 2 Proposed 25 level asymmetric multi- cell CMLI

TABLE I

SWITCHING TABLE FOR PROPOSED SYSTEM

Voltage	Switches
0V	S1, S3, S5, S7
26V	S1, S2, S5, S7, S10
52V	S1, S2, S5, S7, S9
78V	S3, S4, S5, S6, S9, S12
104V	S3, S4, S5, S6, S10, S12
130V	S1, S3, S5, S6, S12
156V	S1, S2, S5, S6, S10, S12
182V	S1, S2, S5, S6, S9, S12
208V	S3, S4, S5, S6, S9, S11
234V	S3, S4, S5, S6, S10, S11
260V	S1, S3, S5, S6, S11
286V	S1, S2, S5, S6, S10, S11
312V	S1, S2, S5, S6, S9, S11
-26V	S3, S4, S5, S7, S10
-52V	S3, S4, S5, S7, S9
-78V	S1, S2, S7, S8, S9, S12
-104V	S1, S2, S7, S8, S10, S12
-130V	S1, S3, S8, S7, S12
-156V	S3, S4, S7, S8, S10, S12
-182V	S3, S4, S7, S8, S9, S12
-208V	S1, S2, S7, S8, S9, S11
-234V	S1, S2, S7, S8, S10, S11
-260V	S1, S3, S7, S8, S11
-286V	S3, S4, S7, S8, S10, S11
-312V	S3, S4, S7, S8, S9, S11

In this system, the input supply to the system is 26V, 26V, 130V, 130V. There are a total of 312 volts. There are total of two bridge circuits, each bridge have two inputs and the first bridge circuit consists of inputs as 26V and 26V, whereas second bridge circuit of 130V and 130V respectively. The first arm of the first bridge is considered as the positive load terminal. The second arm from the first bridge is

connected to the first arm of the second bridge circuit. The second arm of the second bridge circuit is the negative load terminal.

The proposed system is operated in 25 modes and these are controlled by changing the switching periods of the switching devices (IGBT). The table showing the intervals of the switching at different levels of voltages is shown in table I. The different modes operation is represented as following.

The above table I shows the switching operation of the switches. Each switch is designed to operate at the particular time intervals and at particular voltage levels so as to obtained desired output.

IV. NEWLY PROPOSED SYSTEM

In this newly proposed system 85 level Asymmetrical Multi-cell CMLI is presented. By this newly proposed system the THD value is reduced compared to the Existing and Proposed system. By using this topology here Harmonic distortion value is reduced when compared to the Existing and proposed system.

By using other topologies, as the levels were increased simultaneously number of switches were also increased which may increase the switching losses that decreases the efficiency and life span is also decreases. Hence the main reason for using this topology is to improve the fundamental component and also to decrease the THD value and to get the staircase wave form. The 85level asymmetric multi-cell CMLI is as shown in Fig.3.

In this system, the input supply to the system is 7.76V,7.76V, 38.80V, 38.80V,116.4V, 116.4V. There are a total of 325.25 volts. There are total of three bridge circuits, each bridge has two inputs and the first bridge circuit consists of inputs as 7.76V and 7.76V, whereas second bridge circuit of 38.80V and 38.80V and third bridge circuit of 116.4V and 116.4V respectively. The first arm of the first bridge is considered as the positive load terminal. The second arm from the first bridge is connected to the first arm of the second bridge circuit. The second arm of the second bridge circuit is connected to the first arm of the third bridge. The second arm of the third bridge is the negative load terminal.

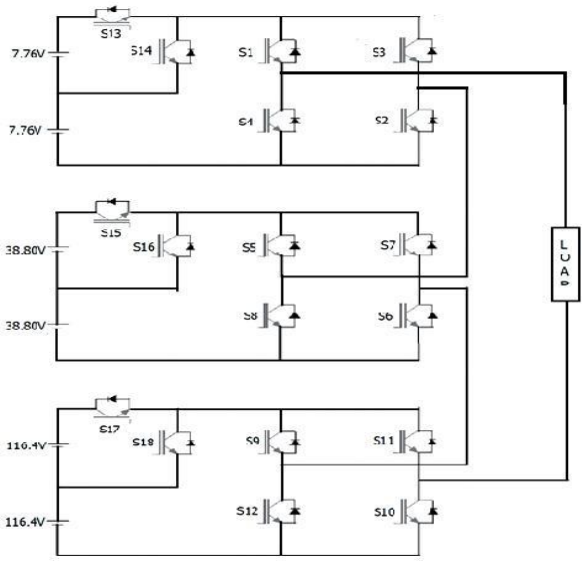

Fig. 3 Newly proposed 85 level Asymmetric multi-cell CMLI

TABLE II

SWITCHING TABLE FOR NEWLY PROPOSED SYSTEM

Voltage	Switches
0V	S1,S3,S5,S7,S9,S11
7.76V	S1,S2,S5,S7,S9,S11,S14
15.52V	S1,S2,S5,S7,S9,S11,S13
23.28V	S3,S4,S5,S6,S9,S10,S13,S16
31.02V	S3,S4,S5,S6,S9,S11,S14,S16
38.80V	S1,S3,S5,S6,S9,S11,S16
46.56V	S1,S2,S5,S6,S9,S11,S14,S16
54.32V	S1,S2,S4,S6,S9,S11,S13,S16
62.08V	S3,S4,S5,S6,S9,S11,S13,S15
69.84V	S3,S4,S5,S6,S9,S11,S14,S15
77.6V	S1,S3,S5,S6,S9,S11,S15
85.36V	S1,S2,S5,S6,S9,S11,S14,S15
93.12V	S1,S2,S5,S6,S9,S11,S13,S15
100.88V	S3,S4,S5,S7,S9,S10,S13,S18
108.64V	S3,S4,S5,S7,S9,S10,S14,S18
116.4V	S1,S3,S5,S7,S9,S10,S12,S18
124.16V	S1,S2,S5,S7,S9,S10,S15,S18
131.92V	S1,S2,S5,S7,S9,S10,S13,S18
139.68V	S3,S4,S5,S6,S9,S10,S13,S16,S18
147.44V	S3,S4,S5,S6,S9,S10,S14,S16,S18
155.2V	S1,S3,S5,S6,S9,S10,S16,S18
162.96V	S1,S2,S5,S6,S9,S10,S14,S16,S18
170.72V	S1,S2,S5,S6,S9,S10,S13,S16,S18
178.48V	S3,S4,S5,S6,S9,S10,S13,S15,S18
186.24V	S3,S4,S5,S6,S9,S10,S14,S15,S18
194V	S1,S3,S5,S6,S9,S10,S15,S18
201.76V	S1,S2,S5,S6,S9,S10,S14,S15,S18
209.52V	S1,S2,S5,S6,S9,S10,S12,S14,S18
217.28V	S3,S4,S5,S7,S9,S10,S13,S17
225.04V	S3,S4,S5,S7,S9,S10,S14,S17
232.8V	S1,S3,S5,S7,S9,S10,S17
240.56V	S1,S2,S5,S7,S9,S10,S14,S17
248.32V	S1,S2,S5,S7,S9,S10,S13,S17
256.08V	S3,S4,S5,S6,S9,S10,S13,S16,S17
263.84V	S3,S4,S5,S6,S9,S10,S14,S16,S17
271.6V	S1,S3,S5,S6,S9,S10,S16,S17
279.96V	S1,S2,S5,S6,S9,S10,S14,S16,S17
287.12V	S1,S2,S5,S6,S9,S10,S13,S15,S17
294.88V	S3,S4,S5,S6,S9,S10,S13,S15,S17
302.64V	S3,S4,S5,S6,S9,S10,S14,S15,S17
310.4V	S1,S3,S5,S6,S9,S10,S15,S17
318.16V	S1,S2,S5,S6,S9,S10,S14,S15,S17
325.92V	S1,S2,S5,S6,S9,S10,S13,S15,S17

The proposed system is operated in 85 modes and these are controlled by changing the switching periods of the switching devices. The table showing the intervals of the switching at different levels of voltages is shown in table II. The different modes of operation are represented as following the table II determines which switches on and off in each level. For example, to get 0V as the output the switches like S1, S3, S5, S7, S9, S11 are triggered. Like that to get the 43th

mode 325V as the output, the switches are S1, S2, S5, S6, S9, S10, S13, S15, S17 are triggered. Hence the current path will be written as 116.4V → -116.4V → S17 → S9 → S6 → - 38.80V → 38.80V → S15 → S5 → S2 → -7.76V → - 7.76V → S13 → S1 → LOAD → S10 → 116.4V then the output will be V0= 325.95V. The THD of the newly proposed multi-cell CMLI is very low because the output can get 85 levels in its staircase waveform. Here total levels obtained is 85 in the positive half cycle and in the negative half cycle are attained and also LC filter values are L=90mH C=55µF and R=70ohms are used. To get the THD value are measured.

V. SIMULATION RESULTS

A. Existing System

In this existing system, seven level inverter with PWM modulation is presented. The Simulink diagram of the existing system is as shown in Fig. 4

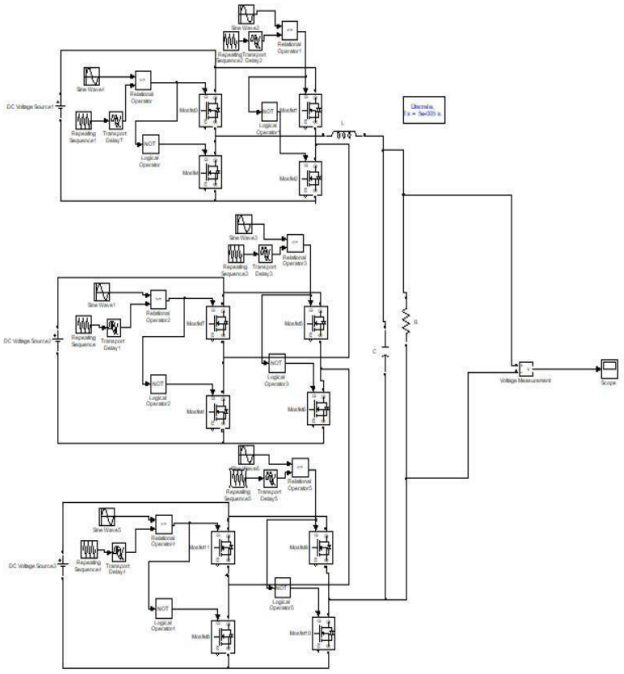

Fig. 4 Simulink diagram of existing system

The input given to the 3 bridges is 300V. So, the output waveform with a peak of 300V is as shown in fig.5 here clearly the output waveform has seven levels as the steps of 100V, 200V, 300V which is shown in below Fig. 5

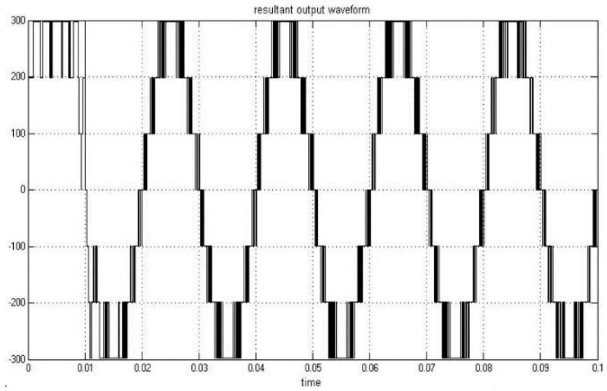

Fig. 5 Seven level Resultant output voltage waveform

B. Proposed System

The Simulink diagram of the proposed system is as shown in Fig. 6

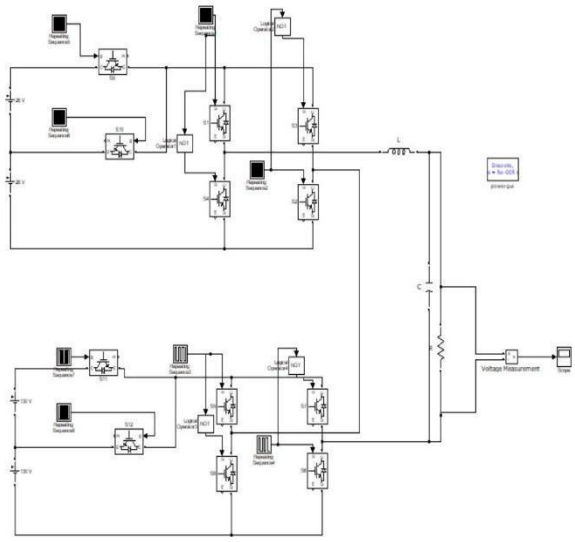

Fig. 6 Simulink diagram of proposed system

The maximum input voltage given to bridge 1 is 52V. Hence the inverter 1 output waveform with a peak of 52V is as shown in Fig. 7

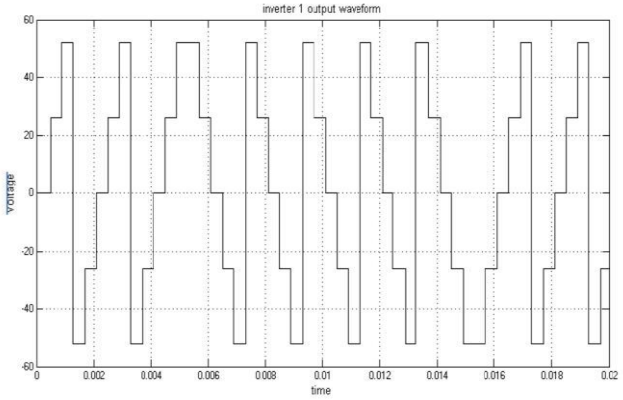

Fig. 7 Inverter 1 resultant output voltage waveform

The total input voltage given to the bridge 2 is 260V then the output waveform of the inverter 2with a peak of 260V is as shown in Fig. 8

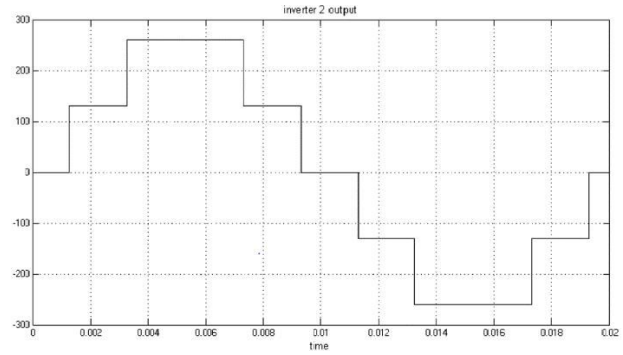

Fig. 8 Inverter 2 resultant output voltage waveform

The total input voltage given to the total circuit is 312V. hence The resultant output voltage waveform of 25 level asymmetric multi-cell CMLI with peak of 312V is shown in Fig. 9

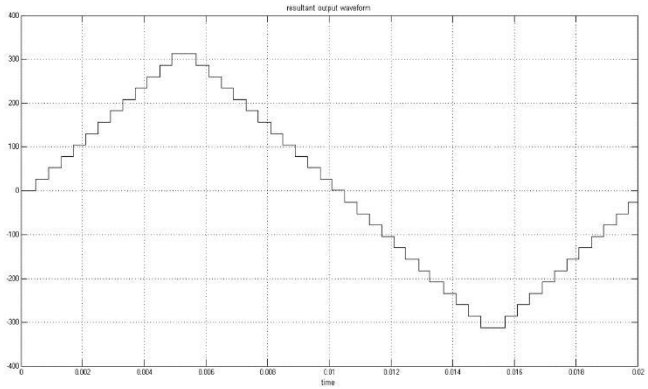

Fig.9 25 Level Resultant output voltage waveform

C. Newly Proposed System

The Simulink diagram of the newly proposed system is as shown in Fig. 10

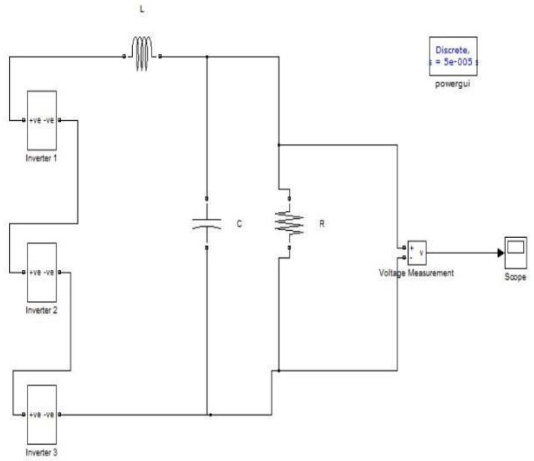

Fig. 10 Simulink diagram of newly proposed system

The inverter 1 output voltage waveform is as shown in Fig. 11the total input given to the first bridge is 15.52V. Hence the obtained peak was 15.52V.

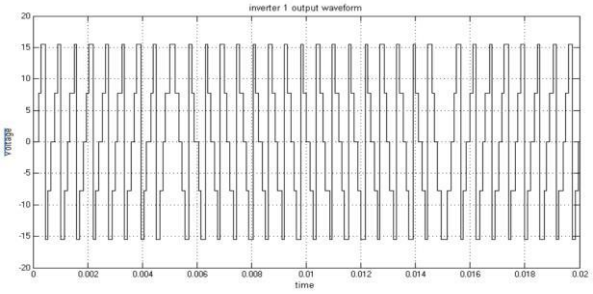

Fig. 11 Inverter 1 resultant output voltage waveform

The inverter 2 output waveform with a peak value of 77.6V is as shown in Fig. 12

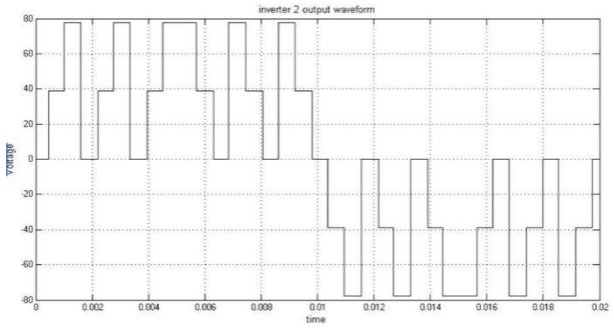

Fig. 12 Inverter 2 resultant output voltage waveform

The total input of the third bridge is given as 232.8V. Hence the output can have peak voltage is 232.8V which is shown in the Fig. 13.

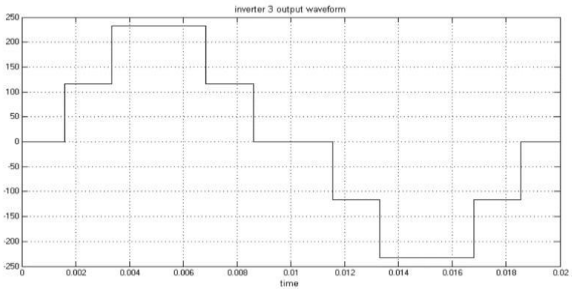

Fig. 13 Inverter 3 resultant output voltage waveform

The resultant output voltage waveform of 85 level asymmetric multi-cell CMLI with a peak of 325.25V is as shown in Fig. 14

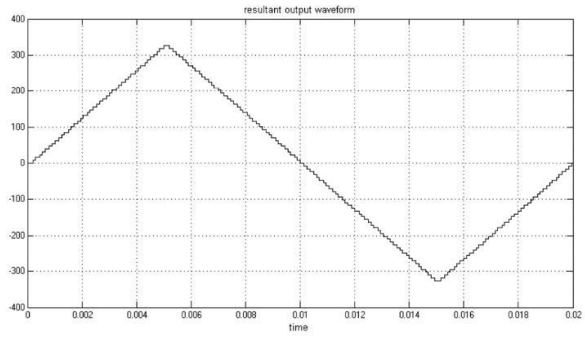

Fig. 14 85 Level Resultant output voltage waveform

VI. FFT ANALYSIS

A. Existing System

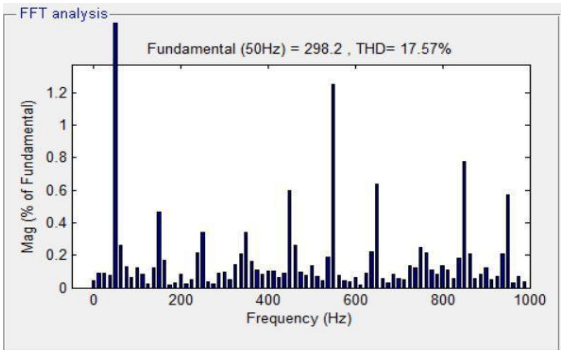

Fig. 15 THD of existing system without LC filter

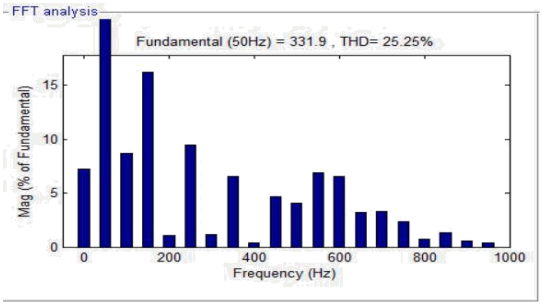

Fig. 16 THD of existing system with LC filter

B. *Proposed System*

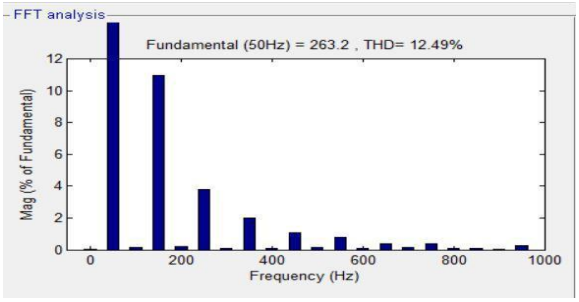

Fig. 17 THD of proposed system without LC filter

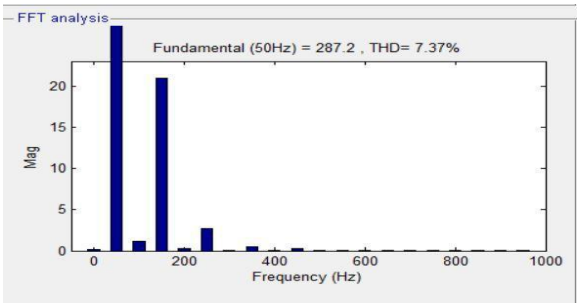

Fig. 18 THD of proposed system with LC filter

C. *Newly Proposed System*

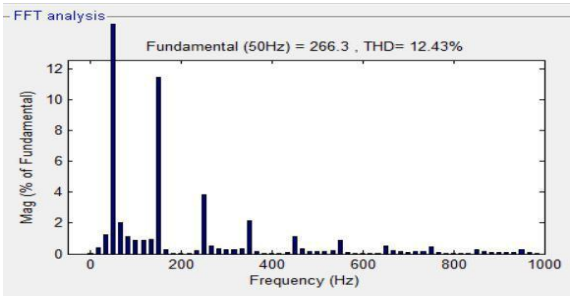

Fig. 19 THD of newly proposed system without LC filter

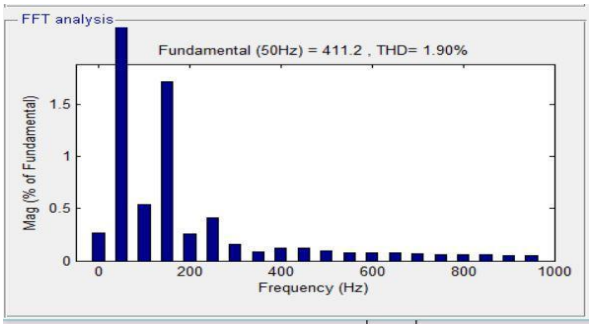

Fig. 20 THD of newly proposed system with LC filter

TABLE III
THD COMPARISION TABLE OF THREE SYSTEMS

SYSTEM	THD without LC filter (%)	THD with LC Filter (%)
Existing system	17.57	25.25
Proposed system	12.49	7.37
Newly proposed System	12.43	1.90

Hence this is the best topology to reduce the THD value (1.90%) in easier way

VI. CONCLUSION

Finally, paper work is carried out on existing system of 7 level with PWM technique, proposed system of 25 level asymmetric multi-cell CMLI and newly proposed system of 85 level asymmetric multi-cell CMLI were presented. The THD value achieved by existing system is 25.25% and by the proposed system of 25 level the obtained THD value is 7.37%. However asymmetric configuration can produce higher number of output levels and there by qualitative output waveform could be generated Thus complexity and voltage balancing issues can be reduced. Here THDs of all the three systems are compared finally by using the newly proposing topology the THD value reduced to 1.90%.

REFERENCES

[1] Babaei E, Alilu S. "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge". *IEEE Trans Ind Electron* 204;61(8):3932-9.

[2] Malinowski Mariusz, Gopalkumar K, Rodriguez Jose, Pe'rez Marcelo A. "A survey on cascaded multilevel inverters". *IEETrans Ind Electron* 2010;57(7):2197-205.

[3] Wu JC, Wu KD, Jou HL, Xiao ST. "Diode-clamped multi-level power converter with azero-sequence current loop for three-phase three-wire hybrid power filter". *Elsevier JElectrical power systems Res* 2011;81(2):263-70.

[4] Khoucha Farid, Laguon Mouna Soumia, Kheloui Abdelaziz, Benbouzid Mohamed El Hachemi. "A comparision of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives".*IEE Trans Energyconvers* 2011;26(1):64-72.

[5] Ebrahimi J, Babaei E Gharehpetian GB. "A new topology of cascaded multilevel converters with reduced components for high-voltage applications". *IEE Trans Power Electron* 2011;26(11):3119-30.

[6] Esfandiari Ehsan, Marium Norman Bin. "Experimental results of 47-level switch-ladder". *IEE Trans Ind Electron* 2013;60(11);4960-7.