AN FPGA IMPLEMENTATION OF SCFDMA USING WIRELESS NETWORK SYSTEMS

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Abstract- In wireless communication SC-FDMA is wide a vital role in the unified network systems. The real time transceivers are using in Single Carrier Frequency Division Multiple access (SC-FDMA)
Signalling system. The transceiver is implemented on a field programmable gate array using Xilinx system generator for DSP applications. in all the blocks are to be needed for the transmission path of SCFDMA.
The transmitter mount can be configured for different
Flier and data schemes. In receiver side, time domain
Synchronization is attained throughout a joint hood
Symbol setup time, hold time, minimization period. And carrier frequency offset signal elevator through the fired information confined in the cyclic prefix.in a least square channel information rescues the channel formal information and a simple zero forecasting scheme has to be implemented for the equalization of the channel information. Results to be showed in implementation of the signal path can be implemented by using the Xilinx system generator for DSP.
Keywords*-SCFDMA; FPG ;Frequency; time domain synchronization; Square channel estimater .*

I. INTRODUCTION

FDMA (Frequency Division Multiple access) is the division of the frequency band allocated for wireless cellular telephone communication into channels. Each of which can carry a conversation or, with digital service, carry digital data. FDMA is a basic technology in the analog advanced mobile phone system (AMPS), the most widely-installed cellular phone in all over country. FDMA each channel can be assigned to only one user at a time.

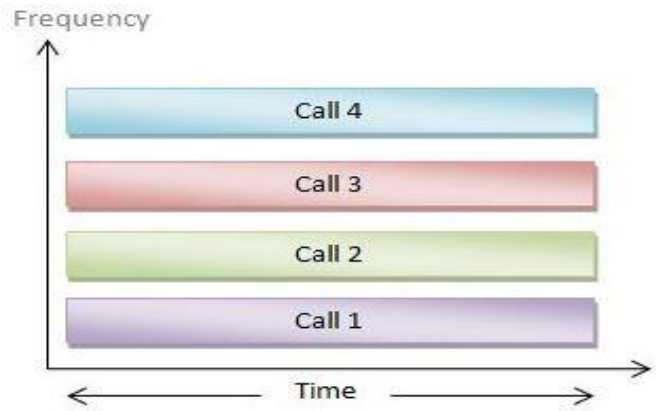

Fig.1: Mobile channel communication

FDMA is one way method of more than one user to share the single radio frequency (RF) spectrum. it's will be done by the all active users in different frequency channels. Track defined ratio (TDR) is the both popular direction of research to the modern communication and key technology of the 5G communications. Now a days green
communications is plays a spirited role in wireless communication network.

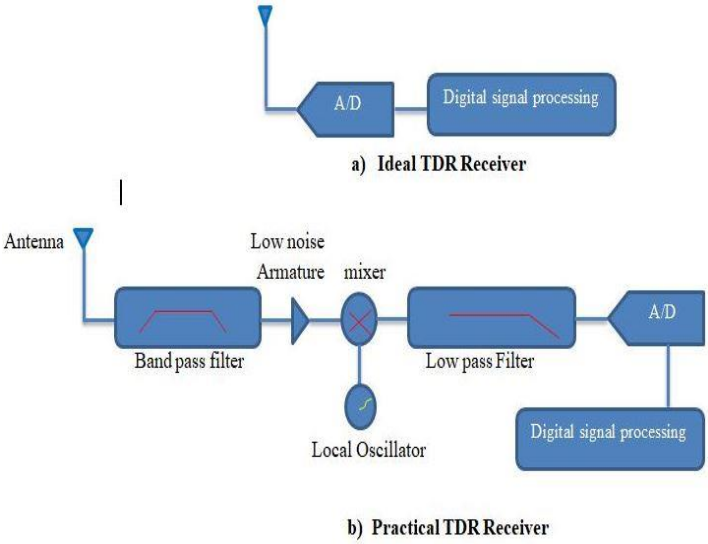

Fig.2:Track Defined Ratio Architecture

TDR is changing towards the ideal and feature TDR's to be replacing with an intelligent system controlled front end RF. it controls the range of the communication system in the mein while of modulation techniques, filtering, frequency bands and bandwidths aiding its flexibility to numerous wireless canons . The Digital-Advanced Mobile Phone Service (D-AMPS) also uses FDMA but adds time division multiple access (TDMA).
TDR's Reconfigurable to allow the programmability of the standard structure to build an extra hardware is to be added to the basic module. In FPGA's (field programmable gate arrays) Gate array - a custom VLSI circuit consisting of huge number of unconnected gates. Circuit functioning is to be determined at the field by the user. Pre-tested for manufacturing defects. FPGA's are having Re-programmable logic components, Re-programmable routing resources and Re-programmable I/O blocks.

In QPLC's are Pre-laid clock trees, integrated big RAM blocks, DLLs, Embedded CPU cores, Special I/O's and Mathematical functions.

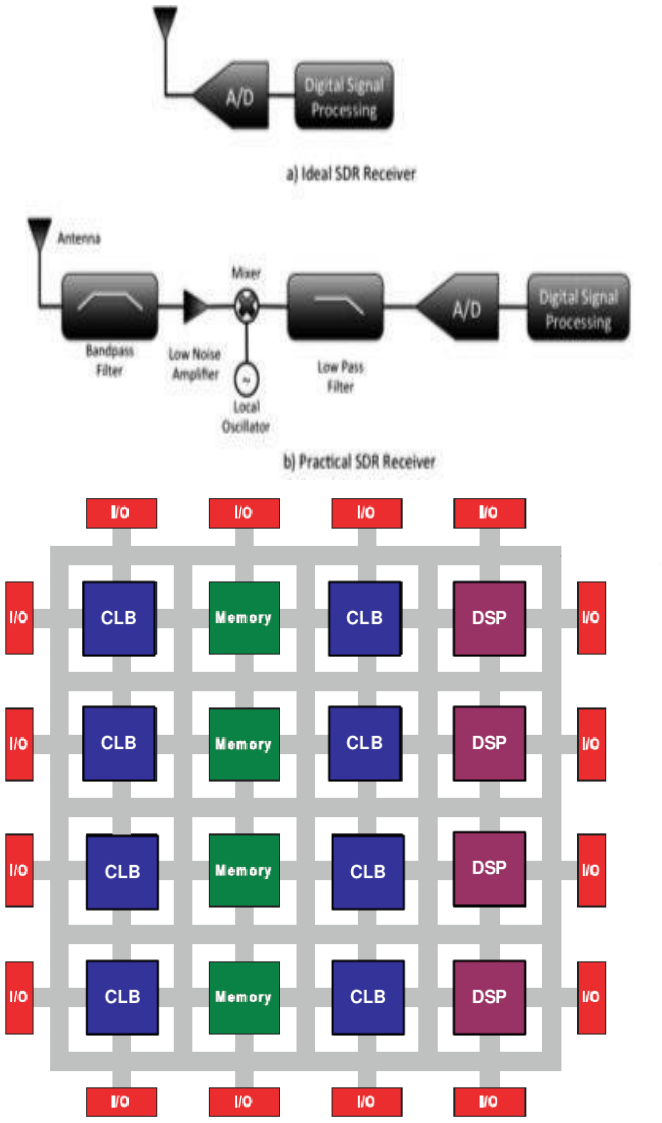

Fig.3: FPGA Structure

Present-day FPGA purveyors include Xilinx FPGA, Altera FPGA, Micro semi FPGA, Lattice FPGA, Tabula FPGA, Quick Logic FPGA among others. Each purveyor has follows its own architectural design approach. A FPGA, see Figure 3, is a reconfigurable logical device involving a group of small logic blocks are to be distributed in a interconnection of array elements. They provide a high computational power while comparing to the other processors.

In Digital signal processing, the audial range providing by a floating point representation, most of the cases fixed-point representation on DSPs and FPGAs are to be provide by a hefty speed and cost value owing to their keen cores. Static apropos process speed, once consecutively a package on a GPP it has various fixed-point swell/hoard cores formerly they were be a far-faster in fixed-point. To comparing the other chips a standard x 86 chips may be slower in fixed point. A floating point depiction will be having a high accuracy rate.

The advance of wireless systems is a long-lasting process that comprises many phases, and then at certain point, corroboration on a hardware test is needed to validate a theoretical and simulation work. Such test beads are used not only for theory verification, but they were also some concepts that can only be truly studied in practice (for e.g., interference modelling).

In a distributed antenna, the radio signals are equally process at a mid-point, therefore the enabling co-efficient interference modification, space diversity besides identical coverage esoteric the cell. Newly, some of the practical centralized pre-coding schemes are to be employed in the painstaking platform. Two centralized multicellular pre-coding schemes based on the water filling technique have been proposed. These techniques are to be achieving a close to the optimal weighted parallel interference cancellation algorithm. A blocking cell optimization (BCO) supportive multi-cell scheme was proposed in [11], the weighted sum-rate attainable for all the user stations (US's) is exploited. A auspicious unified pre-coding structure centred on Zero-Forcing (ZF) condition through numerous power distribution approaches, to reduce the average BER and signal-to-noise ratio (SNR) was proposed in [13]-[14].

The main object of this paper is to implementation of an FPGA based single carrier frequency division multiple accesses (SC-FDMA) receiver with a frequency domain, time domain synchronization using the Xilinx ISE Design suite and Xilinx system generator for DSP processors. System generator will be follow the high-level of abstractions built into Mat lab. The system will be automatically compiled into an FPGA.it provides a user defined primitives of a boundary between software and hardware, it will enables to the hardware design through allowing logical blocks will be synthesize into Verilog and compile them into FPGA.

II. BACKGROUND AND RELATED WORK

SCFDM is a single carrier bandwidth efficiency scheme used in digital communications, The main difference is conventional frequency domain multiplexing (FDM) is that frequency domain of the SC-FDMA sub-carriers overlap to each other, providing spectrum efficiency.SC-FDMA operations are conceded into a digital field, there are more platforms able to design an SC-FDMA system suitable for TDR development.

TDR can be recognised between two main fields: hardware fields and software field. The hardware features of an TDR consist radio frequency parts and communication contacts to the software-based signal processing. The lasting parts will be composed in a DSP's, FPGA.

The Tera-ASIC is chooses Enyx to propose ultra-low latency growth structure and design facilities for their latest FPGA platform. Here we are using the DE2i-150 board it's having the four modules each module associate a multiplicity of Altera Cyclone-IV, letting the provision of 30 million of gates design for each module.it runs logic up to 700 MHz in the digital communication speed at 720 Gbps per module, along through a lithe expansion such as HDMI.it explores the large amount of the data will be possess parallel. Similarly most of

the systems are to be implemented for a design flow model in the process of system generation.

In the view of Software architecture, GNU & C++ is open-source [4] software development toolkits distributed under the General Public License.it provides a set of audio signal processing library's to implementation of the processing blocks are required to transmits the sub- system.it runs only on Linux-based machine processing platform. In graphical flow of the systems they used python programming language.

To implement the RF communication systems one external hardware is rapidly used in communications. An SC-FDMA modulation/demodulation having two synchronization options and error-regulatory techniques is described in [6]-[9]. The working process of SC-FDM signals with Quaternary Phase Shift Keying (QPSK) and Binary Phase Shift Keying (BPSK) modulation technics are to analyse the package ratio used for eminence service process. To design a super-position technique of SC-FDMA systems are used in GNU Radio processing in FPGA [11]-[13] modulators using the Xilinx ISE suite for the DSP based level designs are to be found[14]-[15].

III. THE SINGLE CARRIER FREQUENCY DIVISION (SC-FDMA) MULTIPLEXING TRANSCEIVER

A. Test bench Architecture

SC-FDMA transceiver of the systems, that data will be generated erratically through an Inverse Fast Fourier Transform (IFFT) of phase shift keying (PSK) sign arrays through 1024 sub-carriers. The cyclic prefix tree is added to the IFFT and symbolic representation is turned into original frames. A Logical look-up conversion is formed by the Digital up conversion block. A DUC is a set of two interpolated filters. They are cosine filters and Half-band filters.

The Direct Digital Synthesize (DDS) and mixer blocks are to be performs translation of frequency into an intermediate frequency and attained by mixing of the frame through DDS. and another translator is used in the Receiver side to transforming signals of the inverse Fourier base band signalling blocks are there in a system. Top-Down conversions of the matched filters are to be performed by a set of similar filters as first one will be used in the transmitter block by using a digital top-down conversion.

When the esteemed offsets of the signals are performed, the frame to symbol and also carrier frequency offset correction blocks implements the reparations. A Fast Fourier Transform (FFT) signals are shifted data into Frequency domain. A lower state channel is applied to recover the esteemed state channel information and zero frequency analyser spread over the valuations.

In both perilous of the receivers are time –domain synchronized and device channel estimation signals of the sub-systems.

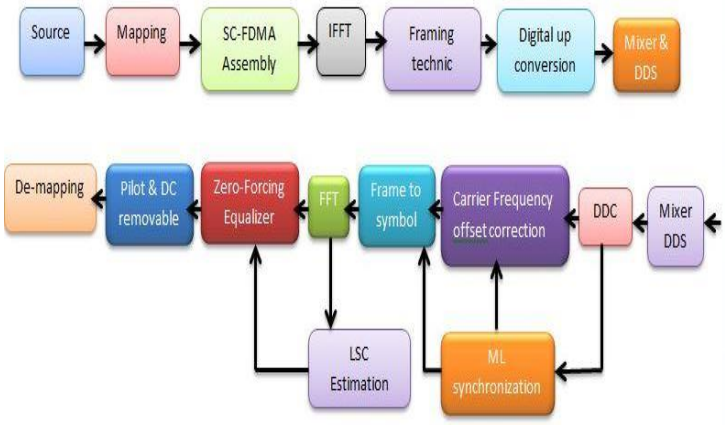

Fig.4: Mapping Architecture of transceiver

Inside the time-domain synchronization process we were calculate the frame levels of time and frequency of equalizer among the resident oscillators and Radio frequency carrier signals. In the carrier channel frequency assessment will be rectified through an equaliser.

B. Peak - Time organisation

In a de-modulation technique, the receiver signals are to be performing a digitalized framing signals and carrier signal synchronization. In order to define the signal synchronization of the phase and frequency among the transition and receiver section. All the sub carrier signals are shifted from the projecting diffusion to pattern plugs.

$G.\square\ x\ \square = k.(x-\tau).e^{j\ 2\pi\epsilon_0 k\ /\ N} + n\ \square\ x$

□□□□□□□→□□□□

Here ϵ_0 is minimized the carrier signal optimization, T is the arrival framing time. k(x) is transmitting signal, N is no.of sampling signals, n(x) is the Gaussian noise, x is the sampling index of each signal up to 1024.

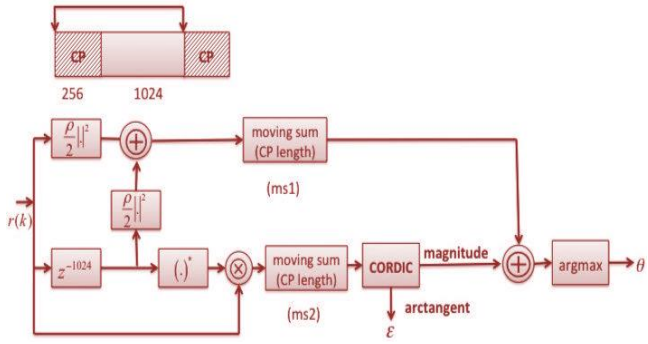

Fig.5: Beek estimation algorithm architecture

We are not using these types of preface conditions on our systems, while we are using aloof structures in each frame for time-domain synchronization owing the auto-correlation assets are given from a part of 3Gpp long term evolution interfaces. In above figure was choosing the design complexity and it's easily changed to take the adoptive gain of aloof systems.

C. Frequency domain channel estimation

Frequency domain channel estimation process will be existing in wireless systems. In this type of wireless systems are braced in the receiver section to eradicate the multi-path phase tracks inside the receiver segment. In SCFDMA systems acquire a precise stands to attain the high possessive spectral density and compactness of demodulation process. Somewhere the frequency response of co-channels by using the discrete sub-carrier frequencies require to accurate esteemed process used in decoding systems. Moreover the synchronization process boons a segment offset register uncertainty later frequency offset correlation must be highly esteemed by the source channel estimator and removing the equalization of system process.

In this process we conferred the uses of circular patterns espoused by the standard LTE with certain variations, here we are taking 24 frame SCFDMA carrier guides in their 1st and 10th and 19th symbol. The carrier guide sub-carriers are optimized and equip-power, equip-distance to achieving the low mean-square error (LMSE).

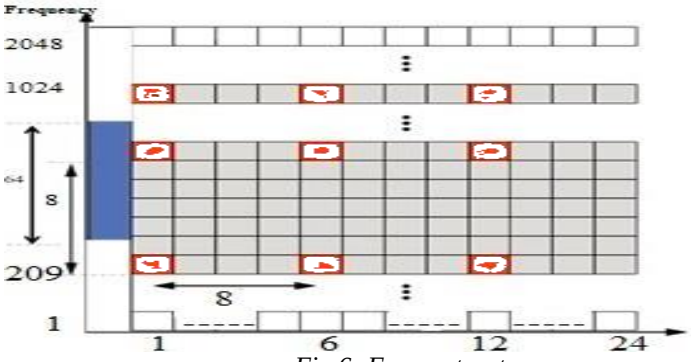

Fig.6: Frame structure

The proper distances of aviators are having 8 subcarriers. In the starting bit and ending bits are not laden building-up of the band Pickets on each and every gamut to comprise the phantom leakage of SC-FDMA systems.

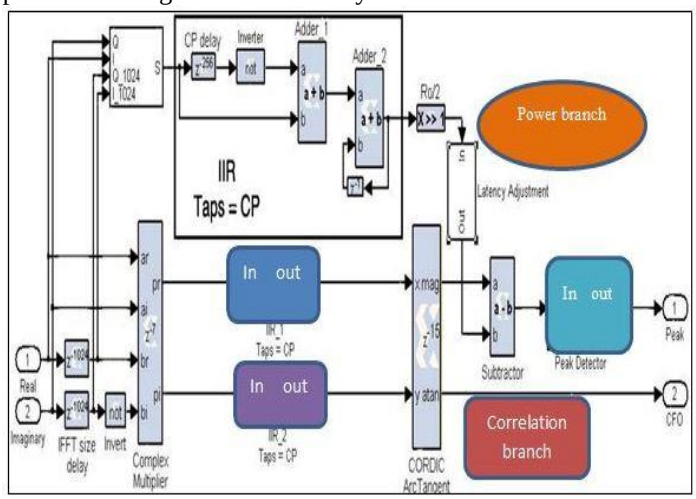

Fig.7: Peak estimation algorithm on Xilinx System Generator for DSP

To overcome these issues to extort the brink of sub-carriers with this subsequence of the assessment accuracy, the espoused framing structure has guides at both brink sub-carriers. In initial stage of work, the guided sub-carriers are using the whole estimator. These conventional estimators are not taking any improvement on the parallel link process the sub-carriers are depends on the time dominie and frequency dominie nor it does across the prior information channel statistics are obtain to estimate, but on another hand to reduce the complexity and requiring the inversion capacity of multiplexing sub-carriers. To check the value of receiving the n^{th} sub-carrier k (n) will be stated as

s□ n□ □ p □ n □ q □ n □ □ k □ n

□□□□□□□□□□□□□□□□□□□□→□□□□

Where q (n) is the effecting channel of the n^{th} sub-carrier. The estimation output channel can be stated as

$$q^{\wedge}(n) = k(n) / p(n) = q(n) + k(n) / p(n) \quad \rightarrow \square\square\square\square$$

that it can be taken as strident sections of the carrier channel frequency interference (CFI).

IV. PEAK ASSESSMENT, FRAME SYNCHRONIZATION AND CFI SYNCHRONIZATION.

In a time domain synchronization algorithm will be divided in to three subcarriers.

A. Assessment of arrival time (T_a) and carrier Frequency (F_c).

In this algorithm is presented on the carrier sub sequent of the framing structure and it's will be adopted from the framing patterns on the above Figure (5). Peak channel feats the carrier frequency interference by comparing with the delayed version. Again a pattern is repeated to detect the arrival framing time and phasing patterns gives to the channel frequency interference.

In this algorithm will showed in the three branches .then first one is to calculating the rising time and second one calculating the falling time and last one calculating the correlation time. These are required to estimate the arrival time and phase offset.

$$Es_1 = \frac{\rho e}{2} \sum_{k=m}^{k+1} \gamma |(I)|^2 + |\gamma(I+N)|^2 \quad \rightarrow (4)$$

$$Es_2 = \frac{JE}{2} \sum_{k=m}^{k+1} \gamma (I) . \gamma * (I+N) \quad \rightarrow (5)$$

Here Equation (4) is to show the calculation of rising time and Equation (5) is to show the calculation of the correlating time. ρ is the magnetic coefficient between γ(I) and γ(I+N) it depends on SNR but it can be set at the same. Both moving sub-carriers are designed by using the Harman filters.

The code multiplier is to boons on system libraries performing the multiply operations during the sub-system. In order to continue the two operations are performed on the foot layer. A composite module generate the peak channel it's to be associate the tardy type and to estimate the angle between the IR signals

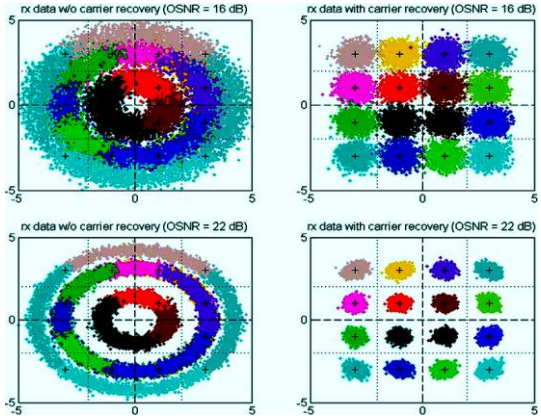

Fig.8: SC-FDMA symbol constellation with rx data
W/o Carrier recovery (OSNR= 16 dB & 22 dB)

In system libraries are providing a Gaussian allusion block that it can be implement a rectangular eclipse direct transformation by using a Gaussian algorithm in globular vector mode, it calculates a magnitude and impious angle equation (6),(7) respectively.

$$|L, P| = \sqrt{L^2 + P^2} \quad \rightarrow (6)$$

$$\text{Avg} = 2\Pi\epsilon_0 = \text{arc}\ (L / P) \quad \rightarrow (7)$$

If assume that the offset between the oscillators are lower than the single sub-carriers. A division operation is accomplished to build the arrival framing detection, but these types of operations in hardware mode is costly that's why it should be avoided. The compiled angle is only way to use find peak is spotted, to conforming the channel frequency interference (CFI) is to use if correlating is ample.

1) Carrier channel Frequency Interference (CFI)

Carrier channel frequency interference is attained with using the Harman filters to executing a switch function.to correlating a vector function (L,P) by angle Φ springy a new functioning a vector(L',P') such that

$$L^{|}(I) = L(I) \times \cos\emptyset - P(I) \times \sin\emptyset \quad \rightarrow (8)$$

$$P^{|}(I) = P(I) \times \cos\emptyset + L(I) \times \sin\emptyset$$

Where, $\emptyset = 2\Pi\epsilon_0 \frac{I}{N}$ $\rightarrow (9)$

By taking the angle it can be attained at section A, if the angle is divided by N samples and each sample can be quashing the phase equalizer of each emblem.

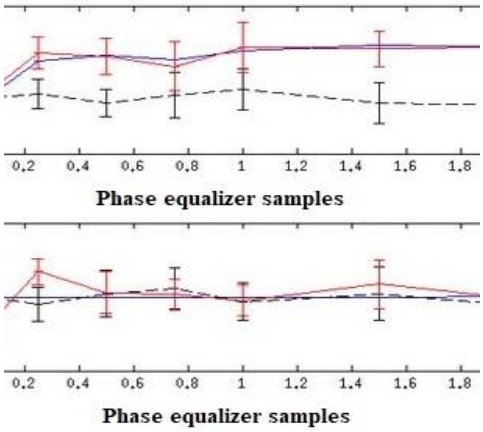

Fig.9: Peak detection phase equalizer samples

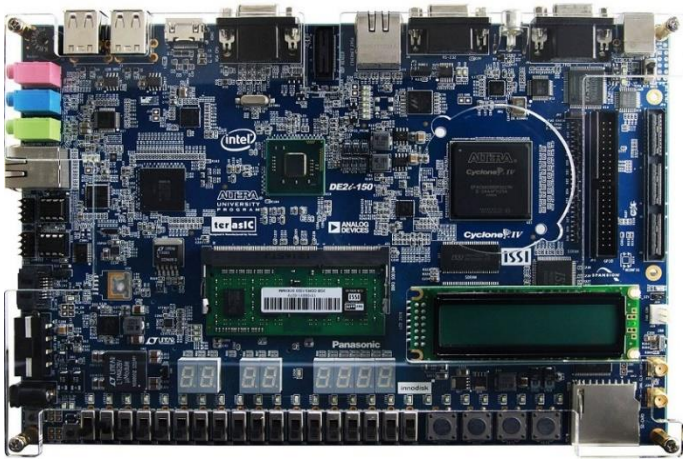

Fig.10: FPGA hardware platform set-up

System Parameters	
Baseband frequency || Bandwidth	20 MHz || 10 MHz
FFT size || CP size	2048|| 512
Modulation	PSK - 16QAM
Subcarrier separation	30 kHz
Symbol duration (Symbol +CP)	68.78 + 18.56 = 87.34 •s
IF sampling frequency	98.64 MHz
Oscillator frequency	30 MHz

Table.1: System parameters

V. SIMULATION & RESULTS

This Design process will be compiled and executed on Xilinx software, which allows a simulation of system to be completely run on Hardware (FPGA) .while showing the results on Modelsim software.it, can be enable to accurate hardware exhibiting along with quick simulation and faster design. This is the easiest way to calculate the hardware verification by implementing the contrived algorithm using the Altera FPGA. In impartial way is to get both Software and Hardware working principles on prototyping stage. In this simulation model was using on the DE2i-150 board is able speed up the responsiveness of the system which contains a Altera Cyclone IV GX FPGA and an On-board USB-Blaster with JTAG and AS mode configuration; 128MB SDRAM; 4MB SSRAM; 64MB Flash and 802.11 b/g/n; Bluetooth 4.0; SSD 64GB; HDMI 1.3a;VGA output see Figure10.

In the test parameters of a wired co-channel systems are run at clock frequency ranges are 98.64 MHZ with an IF of 20 MHZ. The BER hardware results are acquired by using the simlink software. The speculative results are gained from an altered Mat lab SC-FDMA chain.

In Figure 11 illuminate the BER ratio of theoretical and practical effects for four altered simulations: to attain a flawless CSI, there is without time domain synchronization of a RF equalizer and with time domain synchronization of RF equalizer.

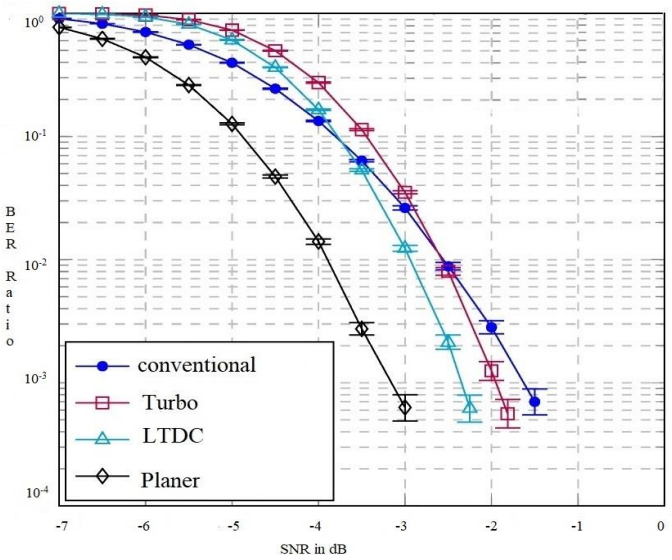

Fig.11: Baseband BER Ratio for 4 simulations

VI. CONCLUSION AND FUTURE SCOPE

A Full baseband signal of RF design was presented focused on the synchronizing and channel estimating algorithm. In this total graft will be performed by using the Xilinx software, chipset pro-tool and validate with Mat lab simulation link. FPGA simulations are possible by using a floating point representation but some of the blocks are functioning on the system libraries to allow such type of floating point operations are used in hardware systems. When the parallel link is occurred the correlated angle should be uttered has a Flat line. But, due to lower Procession will be occurred on fixed point presentation. There are some instantaneous links on the same fixed point line. Our BER results shows that there is no pertinent humiliation between the Mat lab Floating point and FPGA fixed point simulations, we are limiting the bit registers width along with the Floating point algorithm and different system parameters.

In the next stage is to short out the SC-FDMA system generator parameters to words the 5G green communications.

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