ANALYSIS OF DIFFERENT CONFIGURATIONS OF OPAMP

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Abstract— This paper presents the analysis and design of the various configurations of a two stage CMOS operational amplifier (Op-amp). High gain amplifier with DC coupling and differential input usually provides single ended output and is known as Op-amp. Single stage Op-amp is the conventional one and usually provides less gain so two stage Op-amp came into existence to improve gain to a high extent. Two-stage Op-amp consists of differential amplifier in the input stage and the second stage is the gain stage which is also known of common source stage. This paper shows the design analysis of different configuration of two stage Op-amps @ 180nm technology using Cadence Virtuoso and the results of different Op-amps are concluded.

Keywords—*: Miller, OTA, Cascode, Bulk-driven*

I. INTRODUCTION

Operational amplifiers are one of the most popular elements in nearly all electronic systems. Hence designing an efficient Op-amp has become a major need. Various research works are being done to achieve reliable and stable results. Apart from stability and reliability, other parameters such as speed, power, gain, bandwidth, noise etc also plays a vital role in designing the Op-amp. Hence, designing of any Op-amp can be a challenging task. It is often observed a tradeoff between power and bandwidth so Op-amp should be made according to the requirements of any application. Operational amplifiers are one widely used building blocks in mixed signal systems and analog applications too. Therefore, it is essential that output of Op-amps must be stable and should be noise free. Stability of Op-amp is a major concern as if the output is not stable then the results will not be efficient and it keeps on oscillating. Consider step response of second order system as shown in *Fig.1* which shows the closed loop gain of Op-amp. A desired step response is the one which reaches its final value quite early and therefore oscillations should be less which is only possible with high phase margin and therefore its phase margin should be atleast 45 degrees and practically 60 degrees. Phase margin and gain margin are the two parameters that defines the circuit's stability to a great extent. Phase margin is defined as the difference between 180 degree and the phase which is obtained at 0dB gain.

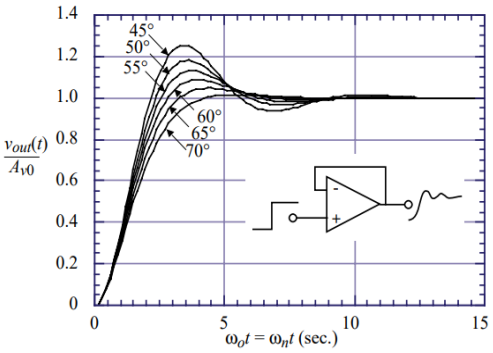

Fig. 1 Graph showing step responses of second order system

Design analysis of any Op-amp is based on the requirements of any circuit. In a single stage Op-amp, there exist only one pole and hence stability is quite less in any circuit. Therefore according to the need in nowadays applications, two stage Op-amps has become a major need and if the design approach of two-stage Op-amp is correct then cascading designs can also be implemented. It can give high output swing and high gain and thus proves to be important for advanced CMOS technologies. Basic block diagram showing the three stages of of a two stage Op-amp is shown in *Fig 2*. Two stage Op-amp shows two poles on the bode plot. The positioning of these two poles plays a vital role in stability of the circuit. The plot shows two poles and these poles should be far part for better stability results. *Fig.3* shows the bode plot for two stage Op-amp.

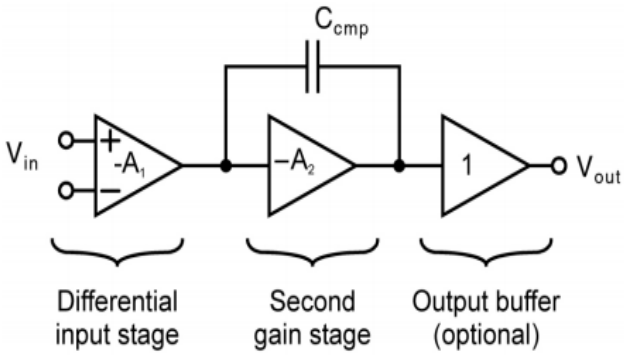

Fig.2 Block diagram of a Two-stage Op-amp

Gain margin is another design parameter and it should always be greater than 1 for better stability. Gain margin acts as a

safety factor for model uncertainty. In simple words, Gain margin describes that particular amount of gain which gets increased or decreased doesn't affect the stability of the circuit. Phase and gain margin should both be high for better results. Now design analysis and circuit diagrams are discussed of different configurations of a two stage Op-amps.

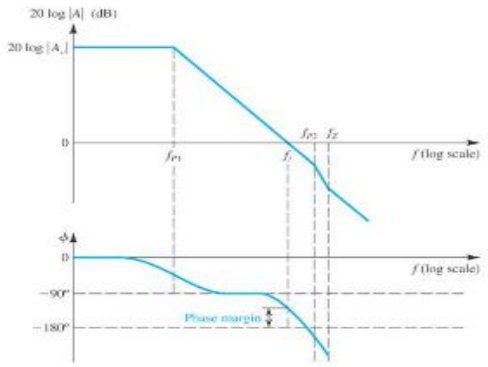

Fig.3 Bode plot of two-stage amplifier

II. DIFFERENT CONFIGURATIONS OF OPAMP

A. MILLER TWO STAGE OPAMP

As the need for two stage Op-amps has already been discussed. So, here is the first Op-amp which is miller two-stage Op-amp. Basically, the miller compensation is provided to achieve better results and high phase and gain margin. In this, the first stage is the CMOS differential amplifier as it is useful in conversion of differential input to single-ended output and also because of its high gain. Input to the circuit are fed from the transistors M1 and M2 which are both NMOS. The first stage is also composed of the current mirror circuit formed by the transistors M3 and M4 which are both PMOS. Now the second stage of the Op-amp is common source amplifier which is made by the transistor M7which is NMOS. The current I_{bias} of the circuit goes to the circuit through current mirrors. Circuit diagram of the Two-stage miller Op-amp is shown in *Fig*. 4.

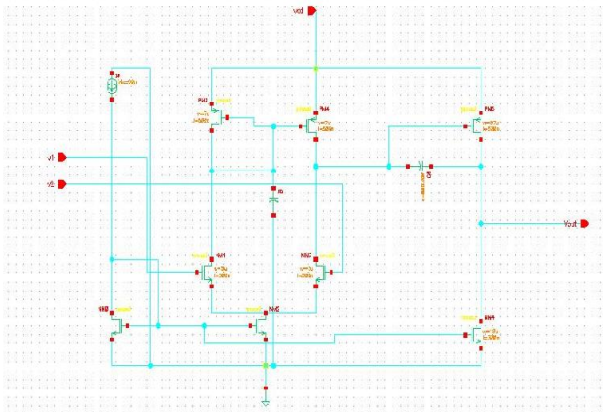

Fig. 4 Two-stage Miller Op-amp.

As shown in figure 3, the second pole should be far away from the first pole to increase the phase margin. If the second pole lies close to GBW then it leads to undesirable results. Design of any Op-amp is basically based on the values of W/L ratio of various transistors which are used in the circuit. These values are found out using various equations. There are 2 poles and 1 zero as obtained from the transfer function of two-stage Op-amp. Value of capacitor load(C_L) plays a major role in calculating phase margin. Here value of C_L is 800pF and W/L ratio of various transistors are given in the Table 1. All the transistors must be in the saturation region which is also known as the region 2. First step in the simulation is to do the DC analysis. DC analysis shows the region of the transistors whether they are in region 1, 2 or 3. It also shows various values of voltages and internal capacitances of transistors. After DC analysis, AC analysis is performed to obtain the desired waveforms.

TABLE 1.

Transistors	W/L ratio
M1,M2	3um/500nm
M3,M4	7um/500nm
M5	2um/180nm
M6	87um/500nm
M7	18um/300nm

B. BULK DRIVEN OPAMP

The second two-stage Op-amp is discussed. Here the differential stage is formed using bulk-driven concept using input devices PM0 and PM4 which are the PMOS transistors as shown in *Fig. 4* . NM0 and NM2 forms active load which actually is a current mirror. Now comes the second stage which is an inverter, here NM1 acts as a driver and PM1 plays the role of an active load. Its output is connected to its input, i.e., to the output of the differential stage using Cc which is the compensated capacitance and is acting as a Miller capacitance and Rc resistance.by means of compensation capacitance C_C in second stage. By setting the Vgs voltage such that transistor may switch on. With this the operation of the Bulk-driven MOS transistor becomes a depletion type. Current flow through the transistor is controlled by applying input voltage to the bulk-terminal of the transistor. Op-amp with Bulk-driven input transistors has been shown in *Fig.4.* Design analysis is important and directly affects the output. W/L ratio of various transistors are 120nm/100nm.

DC analysis verified that all the transistors were in saturation region and after that AC analysis was performed.

The unity gain frequency f_t the Bulk-driven OTA is given by

$$f_{t.} = g_{mb}/2\Pi Cc$$

where $g_{mb} = C_{BS}g_m/C_{OX} = (n-1)\, g_m$.

Note that the low value of g_{mb} causes lower value of unity gain frequency of the Bulk-driven Op-amp .

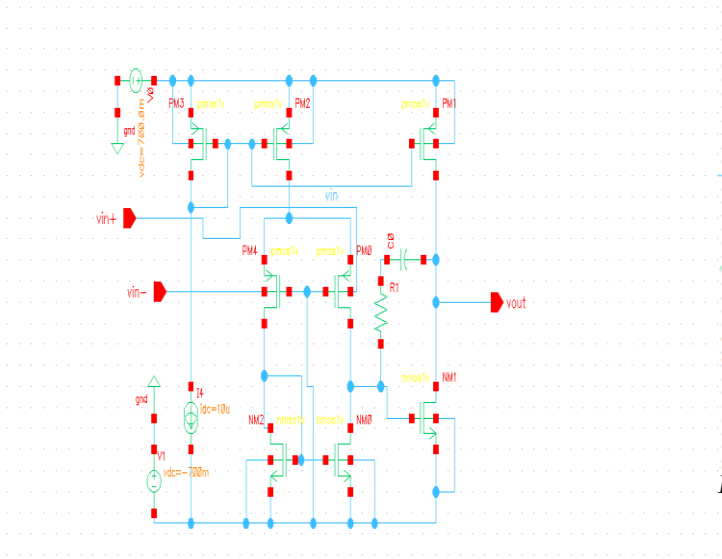

Fig.5 Bulk-Driven Op-amp

C. FOLDED CASCODE OPAMP

Cascode Stage is formed by the combination of common Gate and Common Source stage. As, Op-amps are the basic building blocks in many electronic circuits therefore high gain and high transconductance is required. This can be can be achieved using Cascode stage. It also helps in achieving a constant GBW. Folded cascode configuration is basically the modified form of the normal cascode stage. Normal cascode is formed by the combination of CG-CS stage in series but the main requirement is to use same transistors whether NMOS or PMOS. The main difference is that this configuration consists of two transistors either n channel and p channel or both n channel transistors in a way that both transistors must face each other. Folded cascode Op-amp is more clear from *Fig. 6* . Similarly, it is extended one more time with M3 M4. As described earlier also, W/L ratio plays an important role in designing of the Op-amp. Here, W/L ratio for NMOS and PMOS transistors are kept as 1:2. All the transistors are observed and verified and they are all in saturation region as required. The input voltage given is of 1.2 V. The power supply given is of 1.8 V.

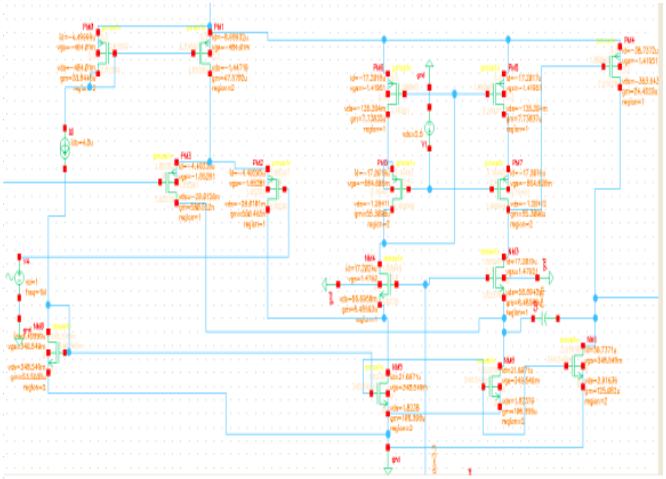

Fig.6 Folded Cascode Op-amp

III. RESULTS AND SIMULATIONS

Now this section shows the results of all the three discussed configurations of Op-amps. Simulations have been done using cadence tool at 180nm technology. Phase margin and gain margin are two vital parameters as discussed earlier, So phase margin and gain margins of Op-amps have been shown.

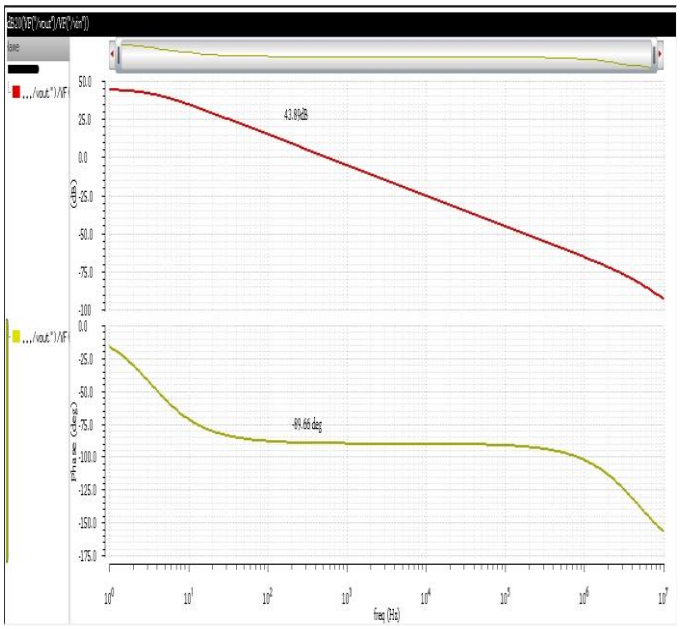

Fig.6 Phase and Gain margin of Miller Op-amp.

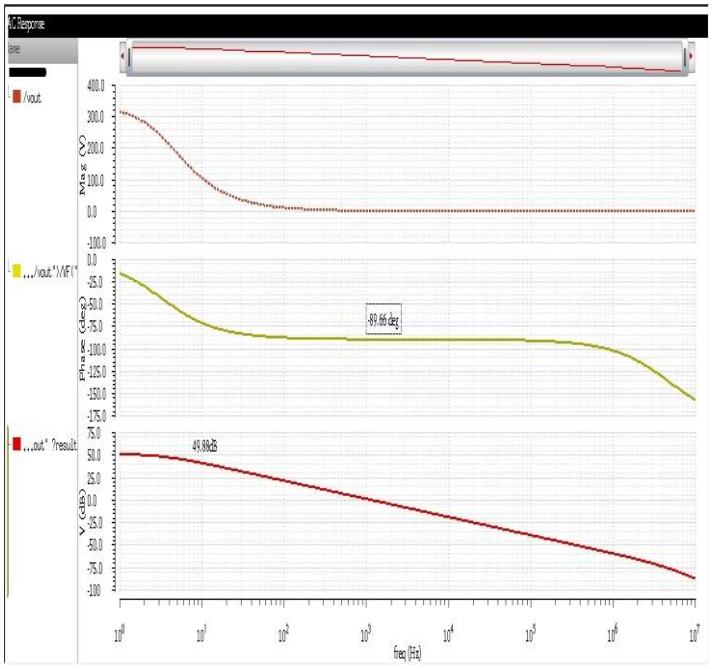

Fig.7 Phase and Gain margin of Bulk-Driven Op-amp

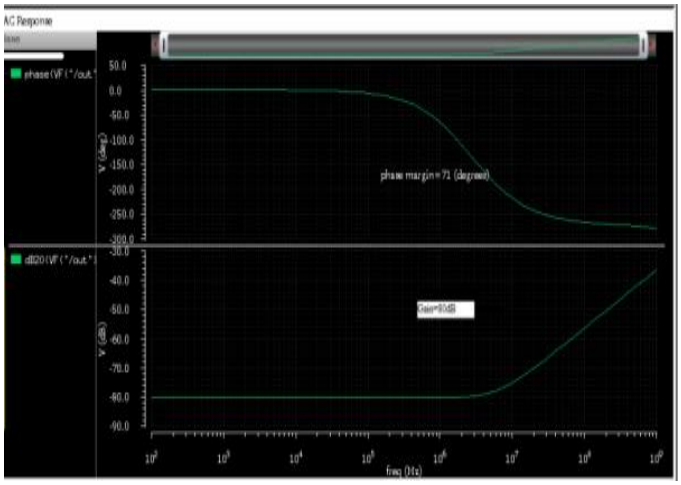

Fig.8 Phase and Gain margin of Folded Cascode Op-amp

IV Conclusion

TABLE II.

Opamp	Phase Margin (Deg)	Gain Margin dB
Miller	89.98	59.12
Bulk-Driven	89.86	53.45
Folded Cascode	71.86	80

It is shown the that W/L ratio is an important parameter in design analysis which ultimately affects the output. High phase and gain margin are the two requirements for opamp. All the three configurations have been discussed and now all the results are compared in the Table II.

III. References

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