A Survey about ADPLL and IoT Applications

J.Jeslin Jijo[1], R.Dinesh[2]
[1]*M.E VLSI design (second Year),* [2]*Associate. Professor/ECE*
[12]*Marthandam College of Engineering& technology, Kanyakumari district, Tamilnadu, India*

Abstract- All Digital Phase Locked Loop (ADPLL) is used as an important component in applications like communication, control system and latest IOT applications. This paper gives the drawbacks of Analog Phase Locked Loop and the importance of Digital Phase Locked Loop and their applications. All Digital Phase Locked Loop contains three important components, namely phase detector, loop filter and Digital controlled oscillator. The different combinations of these three components will give variation in performance, locking range, locking time, power consumption, area etc. The paper also gives the different combinations of components and their effects in the All Digital Phase Locked Loop parameters

Keywords- All Digital Phase Locked Loop (ADPLL), Digital Controlled Oscillator (DCO), Analog Phase Locked Loop (APLL), Digital Phase Locked Loop (DPLL),

I. INTRODUCTION

Phase locked loop is a building block of all synchronization systems .In PLL it adjusts to match the frequency of an input signal and improves the system performance. The analog PLL has high power consumption and large area. In APLL, the phase detector is analog multiplier generates the control voltage. The PLL's are noise sensitive and some are expensive. In order to overcome the drawbacks of these APLL, we go for Digital Phase Locked Loop. In DPLL, the phase frequency discriminator and charge pumps generate control voltage. It may have digital divider in the loop. The noises occur due to quantization error and it does not handle high frequency signals. To overcome these disadvantages we go for All Digital Phase Locked Loop (ADPLL). An ADPLL is also a PLL implemented only by digital blocks. The signals are digital (binary) and may be a single digital signal or a combination of parallel digital signals. It uses delay locked loop rather than VCO for its frequency generation and the control voltage is a bit based. ADPLL achieves a fast frequency locking by using feed forward compensation and also by reusing frequency divider [19]. The ADPLL has the advantages of low power consumption, small area, and small locking time, no off chip components availability and it is insensitive to technology. It is useful in pure CMOS implementation. Bang-bang phase detector (non-linear) is preferred for the design of ADPLL because of its good robustness and the low power consumption [18]

In this paper, we present the role of ADPLL, different combination of components of ADPLL and applications.

The paper is organized as follows. In section II, it describes the surveying of author's contributions about ADPLL. Section III and IV finally present the Inferences about ADPLL and conclusion.

II. SURVEYING

Ahmed Elkholy etal, designed a digital architecture which adopts a narrow range low-power time-amplifier based TDC for achieving sub 1ps resolution. The advantage of this paper is low jitter, low band noise and low power consumption. The main drawback of this method is spurs are produced.

The author Domanic Maurath etal, designed a Frequency Modulated Continous Wave (FMCW) radar system used for the measurements of object positions and velocities. DCO in the ADPLL gives wide frequency tuning range. In this paper, the advantages are most excellent FOM (Figure Of Merit) value, low noise, Power efficient and improved frequency tuning range. The system gives drawbacks such as inefficient bandwidth and improvement in the spurs.

Teerachot siriburanon etal developed the ADPLL using digital sub sampling architecture in voltage-domain digitization. The advantages of this method are low noise performance, low power consumption and multi-bit phase digitization with fine resolution. The drawback of this paper is tradeoff in resolution.

Ao Ba etal, describes the transmitter. for IOT applications The proposed method utilized the Least Significant Bit truncation error for efficiently pre-process the amplitude/phase modulation. A dynamic divider and oscillator is implanted for efficient local oscillator generation. The advantages are less core area, high power efficiency and low fractional spurs level. The drawbacks are the design produces the quantization noise and long delay.

The author Aravind Tharayil etal, design an ADPLL targeted for reducing the noise performance. The proposed method used pipelined phase-interpolator assisted DTC for multiphase generation. The advantages are eliminating phase inaccuracy and low power consumption. The drawbacks of this method are more area, jitter and delay.

Wei-sung chang etal, designed a low noise divider less PLL employing a sub sampling locked loop to perform fractional-N operation. The proposed method used frequency locked aiding circuit for improving the locking range .ADPLL used as a frequency synthesizer has been fabricated in 0.18µm CMOS technology. The system gives low noise, efficient FOM, best

RMS jitter and reduced fractional spurs. The drawbacks are more area utilization and delay.

Xing qiang peng etal, describes an ADPLL based zigbee transmitter. The Zigbee transmitter improves the scalable output power and system efficiency and also reduces the area. A fractional –N ADPLL used a two-point data modulation and class-F DCO-power amplifier. The drawback is noise occurs in high range.

Regarding to the author Dinesh Kumar B, etal designed an ADPLL in CMOS VLSI design circuit. The proposed method utilize a new multiplexer- based frequency selector for obtaining efficient PLL to do frequency synthesis. The drawback of this paper is fast settling time.

The author Feng-Wei Kuo etal, design an ultra low voltage fractional-N ADPLL with single 0.5 supply used for Bluetooth Low Energy. The Process Voltage Temperature (PVT)-insensitive TDC with switched capacitor doubler is used. The ADPLL produces maximum efficiency of 85% and at the same time it reduces the output power. The drawbacks are high area utilization and jitter problems.

For WPAN (Bluetooth dmart and Zigbee) applications, the author Vamshi Krishna Chillara etal, describes the design of ADPLL based ultra low power transceiver. The method used transmission-gate-based dynamic divider and Asynchronous counter implemented in circuitry. The important merits are high speed, low power consumption and low voltage operation. The main drawbacks are RMS jitter and error occurs.

Shahzad Muzaffar etal, introduce the pulsed decimal technique for single-channel, dynamic signaling for IOT applications. The proposed method used pulsed decimal communication techniques and PDC protocol analysis & optimization. The advantages are more reliable and improvement in data rate. The drawbacks are packet failure rate and the area increases.

Japa Aditya etal, design tunneling field - effect transistors based alternative logic gate. The method used Novel logic design exploiting TFET for energy efficient and Tunnel FET based TDC. The advantages are throughput increases and area/energy efficient. The drawbacks are delay will occurs.

For IOT application, the author Ms. Supriya C. Padwal etal says the design of system to monitor the environment of soil with the help of Wireless Sensor Network. The sensors and networking process is done in this method. Features are heat production is reduced, flexible, smart advanced energy management, less human effort, high secure system and easy to install. The applications are area monitoring, Industrial monitoring and earth health monitoring.

Based on the role of IOT in disaster management, the author John Wellington J etal, describes how to minimize the damage and risk involved in disasters by using various technology. Here the method used is disaster management techniques and disaster services. The advantages are risk reduction, community preparedness, shelter and settlement and reduced damage.

Low cost error monitoring for improved maintainability in IOT applications the author Maurico D. Gutierrez etal, describes the design of electronic system with power constrained embedded devices for variety of IOT applications. Here the proposed method used is monitoring techniques design flow, architecture of the signal probability monitors, SEB (Systematic Errornous Behaviour) ranking software. The advantages are area cost reduces and less power consumption. The drawbacks are error occurs and the variation in signal probability occurs.

Table1: Comparison of different ADPLL structures

Sl No	Paper No	phase detector	loop filter	Digital controlled oscillator	power	frequncy range
1.	1	DTC-based bang-bang phase detector	Digital loop filter	LC-based DCO	3.7mW	4.5GHz
2.	3	ADC-Phase Detector	Digital loop filter	18 bit class-c DCO	4.2mW	2.2GHz
3.	7	Phase-frequency detector-charge pump	Digital loop filter	Class F DCO-PA	22.6% at a 0dBm Pout	2.4GHz
4.	8	Phase frequency detector	Low pass filter	Current-reuse Voltage controlled Oscillator	360uW	0.9GHz
5.	5	Phase-Interpolator	Low pass filter	-	3.3mW	4.3GHz to 4.9GHz

III. INFERENCES

For IOT applications, the ADPLL are used in 40nm CMOS technology to reduce the power and to achieve the less phase noise performance. When comparing with other reference papers, the "variable-preconditioned LMS" calibration algorithm is introduced to correct the DTC gain error. By using fractional-N sub sampling digital PLL for Internet of Things applications targeting with Bluetooth Low Energy (BLE) and IEEE802.15.4 standards. Several circuit design techniques such as LSB truncation error feedback are used to efficiently pre-process the AM/PM data to improve the transmitter performance in the IOT applications.

The ADPLL using a voltage-domain digitization realized by the ADC instead of adopting a traditional TDC which can suffer in tradeoff resolution and in power consumption. By employing a sub sampling lock loop, a low-noise divider-less PLL, samples the VCO output by the digital pulse-width modulator to perform fractional-N operation..The author used

ring based oscillator compare to LC oscillator because of its low power consumption IoT's are using with wireless sensor networks for monitoring, gathering information applications such as health care/medical applications,agricultural applications , etc. ADPLL is an essential block in IoT for generating clocks especially in RF transceiver

IV. CONCLUSION

ADPLL utilized in various areas are analyzed. ADPLL can be used for synchronization, modulation, frequency synthesis etc. The different combination of ADPLL components namely phase detector ,loop filter and Digital controlled oscillator will decided the important parameters like loking range, area, power consumption etc.nowdays it is an unavoidable block in IoT applications

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J.JESLIN JIJO obtained her B.E (ECE) from Anna University Chennai. Currently she is doing M.E (VLSI DESIGN) in Marthandam College of Engineering & Technology, (Anna University, Chennai.) Her area of interest includes digital design, VLSI design, etc.

Mr.R.Dinesh has been in teaching for 14 years and currently working as Associate Professor in ECE in Marthandam College of Engineering &Technology, India. He has received the B.E degree in Electronics and communication from Bharathidasan University, India, M.E degree in Optical Communication from Anna University, India and M.B.A degree from Madurai Kamaraj University, India. Currently he is doing PhD in VLSI. He has published 15 technical papers in International conferences and journal in the areas of optical

communication, VLSI and signal processing. He is a life time member of ISTE. His research area of interest include, Low power VLSI, Clock Synchronization, ADPLL etc.