TBS-TR01

고속신호 전송과 문제해결을 위한

Signal Integrity 원리와 측정, 분석 교육

Fundamental of Signal Integrity and High Speed Signal Test

2015년 3월 25일, 서울

Organizer: NUBiCOM

Sponsor: DSFsystem

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Contents

- Introduction of the high speed signal world.
- Characteristic Impedance and Transmission line
- Reflection and termination topology
- Loss, S-parameter and Loss compensation
- TDR measurement
- Differential signal, Differential Impedance, Common mode signal
- Crosstalk
- EYE diagram and Jitter analysis
- Measurement setup(Test Points)

Recent High Speed Signal Standards Trend

Standards	Version	Data rate *	Year	Application
USB	3.1	10Gbps	2014	PC Peripherals
	3.0	5Gbps	2008	PC Peripherals
PCI Express	4.0	16GT/s	2014	Chip to Chip,
	3.0	8GT/s	2010	Chip to Chip, Card
DDR	4	~3200MT/s	2014	Chip to Chip, DIMM
	3	~2133MT/s	2007	Chip to Chip, DIMM
SATA	3.2	16Gbps	2013	Storage
	3.0	6Gbps	2009	Storage
HDMI	2.0	6Gbps	2013	Multimedia(Display)
	1.4	3.4Gbps	2009	Multimedia(Display)
MIPI	M-PHY	5.8Gbps	2011	Mobile, Chip to Chip
	D-PHY	1.5Gbps	2009	Mobile, Chip to Chip
Ethernet	IEEE802.3bq	40Gbps	2013 TF	Backplane, Server
	IEEE802.3bj	25Gbps (40Gb/s&100Gb/s on 4lane)	2011 TF for copper	Backplane, Server

* Transfer on Copper only
* Max .Data rate on a Single channel

What is "High Speed"?

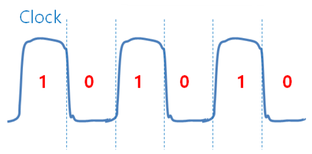
Here, We have basic Questions;

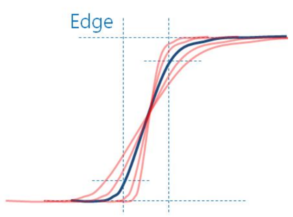
Q: Why do we care about the High Speed/Frequency Signal?

Q: How fast Data rate or Clock Frequency is the "High Speed Signal"?
100MHz Clock? 1Gbps Data?

Basic Terms… on Digital Signal

- Period / Frequency
- Fundamental (harmonic) Frequency
- BPS (Bit per Second); Mbps, Gb/s
- T/s (Transfer per Second); MT/s, GT/s
- UI (Unit Interval)
- Duty cycle
- Rise Time





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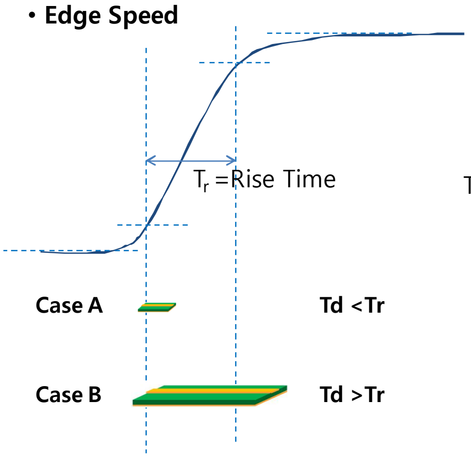
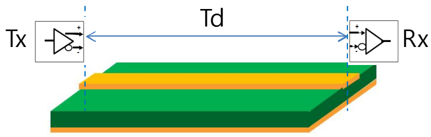
Rise Time and Length of Transmission Line

- **Edge Speed**



- **Time Delay**
(Propagation Delay, Electrical Length)

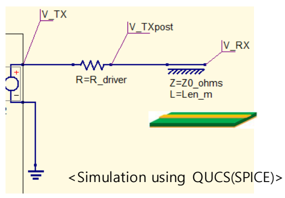


6inch / 1ns (@FR-4 PCB)

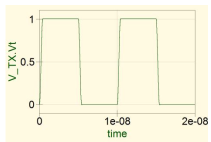
- **Starting point of Signal Integrity consideration**
- **Eg. 100MHz Clock.**

Rise Time and Length of Transmission Line

Without Proper High Speed Design
(Z_0=70ohm, R_{driver}=10ohm)

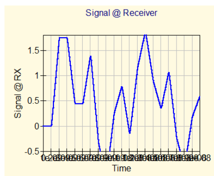


<Simulation using QUCS(SPICE)>

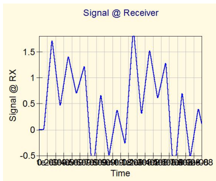


Tx Clock
Freq=100MHz
Tr=1ns

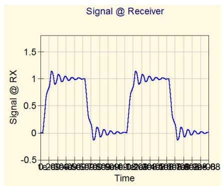
Td of Trace=1ns
100% of Tr



Td of Trace=0.5ns
50% of Tr



Td of Trace=0.2ns
20% of Tr



Rise Time and Length of Transmission Line

6inch / 1ns (@FR-4 PCB)

- 100MHz Clock with **Tr=1ns**
  20% of Tr=Td 0.2ns → Trace >**1.2inch** Length @FR-4 PCB is Critical

- **Tr≒50ps**(0.05ns) ; Commonly used in Today's HS silicons
  20% of Tr=Td 10ps → Trace >**0.06inch** Length @FR-4 PCB is Critical

www.ti.com SLLSE41B – JUNE 2010 – REVISED FEBRUARY 2012

Two-Channel SATA 6-Gb/s Redriver

Check for Samples: SN75LVCP601

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{20\text{-}80TX}$	Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. At 6Gbps under no load conditions	42	55	75	ps

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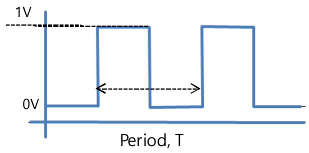
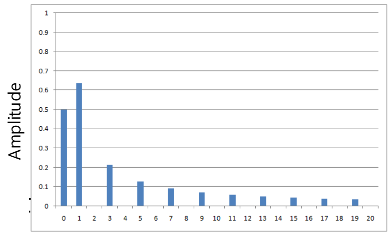
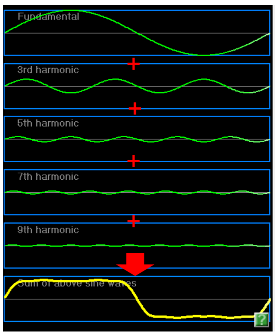
Bandwidth of Digital signals

Ideal square wave and Frequency components(Harmonics)



Frequency= 1 / T





Ideal square wave:
Rise time is "0".
Rise and fall edges are symmetry.
Duty cycle is 50%.
No ringing, no distortion

$$A_n = \frac{2}{\pi \times n}$$

A_n: Amplitude of the nth harmonic
π: the constant, 3.14159...
n: the harmonic numbers, only odd mode

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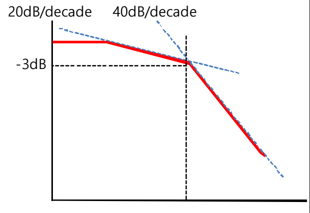
Bandwidth of Digital signals

Rough estimation

1GHz Square wave

5^{th} Harmonic = 5GHz → Bandwidth of this signal



Bandwidth calculated by rise time, more accurate

$$BW = \frac{0.35}{T_r}$$

BW: Bandwidth, in GHz
Tr: rise time 10~90% of edge, in ns
0.35: constant, 0.22 for Tr 20~80%

If Tr ~7% of T=1ns (1GHz)
Tr= 0.07ns(70ps)

→ $BW = \frac{0.35}{0.07}$

= 5GHz

✓ 5^{th} Harmonic estimation method is very accurate when Tr ~ 7% of Period.
✓Constant 0.4 for Tr10~90%, 0.5 for Tr20~80% are used in some test company.

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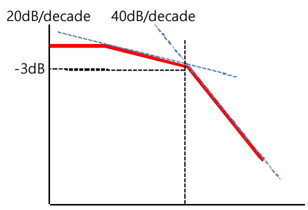
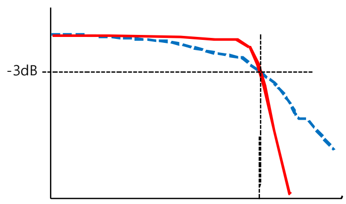
Measurement Bandwidth

Vector Network Analyzer: Specified Instrument BW has 0dB loss.

Oscilloscope and Probes: Bandwidth is specified at -3dB



Bandwidth of Oscilloscope



Bandwidth of Oscilloscope, analog and digital filtered response
Dot plot: analog Gaussian response

✓Method 1: Put the signal bandwidth below -3dB Bandwidth of the Oscilloscope
✓Method 2: With Rise time,

$$Tr_{measured} = \sqrt{Tr_{signal}^2 + Tr_{system}^2}$$

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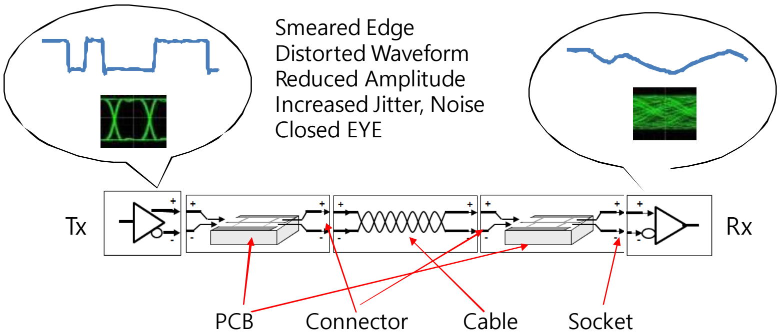
Common Issues of Channel/Interconnects



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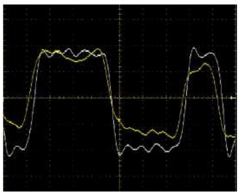
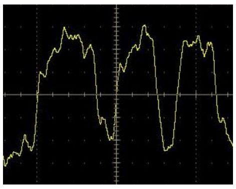
Common Problems of Analog Deviation

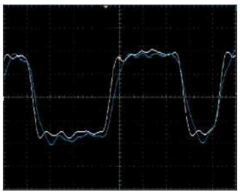


Amplitude Problems

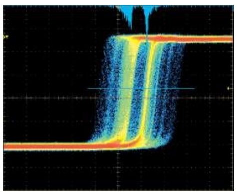
Loss



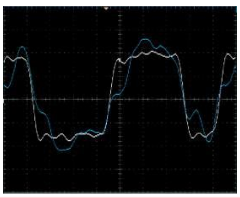
Crosstalk



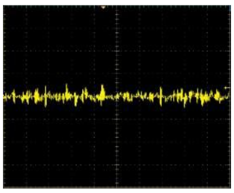
Edge Aberrations



Jitter



Reflections



Ground Bounce

Vcc Noise, Droop

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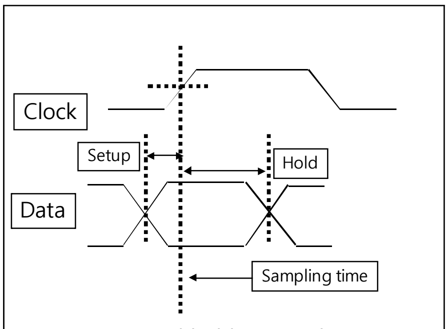
Problems Created by Digital Timing Issues

All Analog Deviation of Clock and Data affect Digital Timing issues

- **Bus contention**
- **Setup and hold violations**
- **Metastability**
- **Undefined conditions**



Setup and hold timing diagram

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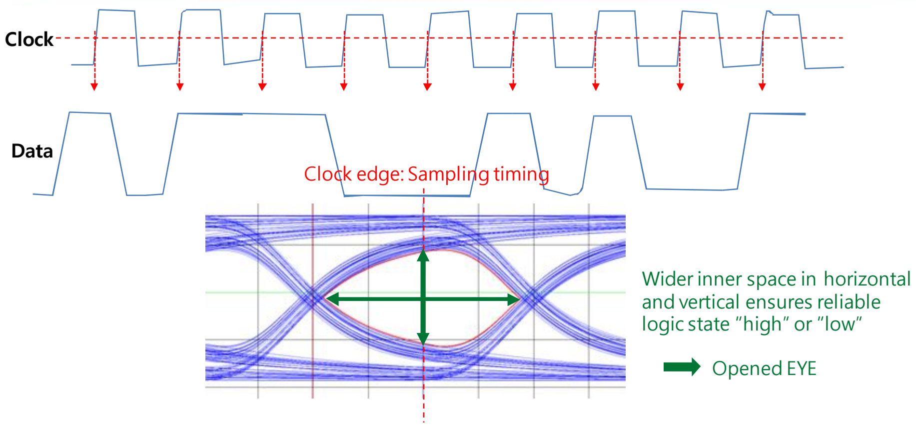
Brief look at the EYE Diagram



EYE diagram(Pattern) is the Integrated view of signal qualities

✓Jitter	✓Setup time
✓Noise	✓Hold time
✓Unit Interval(UI)	✓Rise time
✓Distortion	✓Fall time

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What is Signal Integrity?

Good Signal Integrity of Digital Signal Means:

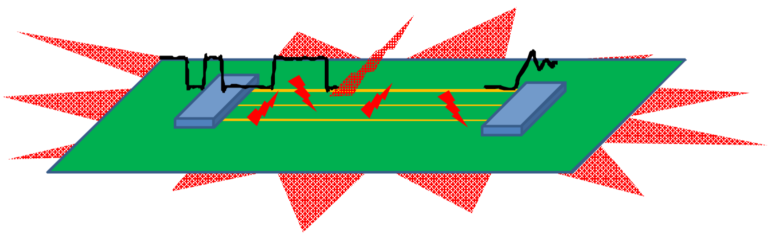
- Clean, fast transitions
- Stable, valid logic levels
- Accurate placement in time
- Free of transients

Examples of Signal Integrity Terms

Characteristic Impedance, Rise Time Degradation, Loss, Emission, Cross Talk, Jitter, Topology, Eye Diagram, Return Current Path, Stub, Reflections, Delay Susceptibility, Power Delivery, Inductance, Ground Bounce, Mode Conversion, Capacitance, Common Mode, Transmission Line, Ringing, Skin Depth, Termination, Coupling, Distortion, TDR, S-Parameter, Dielectric Constant, Differential, Impedance Discontinuity, Inductance

4 Categories of Signal Integrity

1. Signal Quality of one net
2. Crosstalk between multiple nets, ground and power plane
3. Voltage Noise in power distribution network (→Power Integrity)
4. Electromagnetic Interference (→EMI)



Transmission Line & Characteristic Impedance

Transmission Line

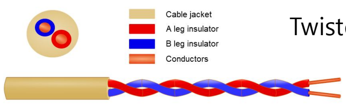
PCB

Microstrip Line

Strip Line

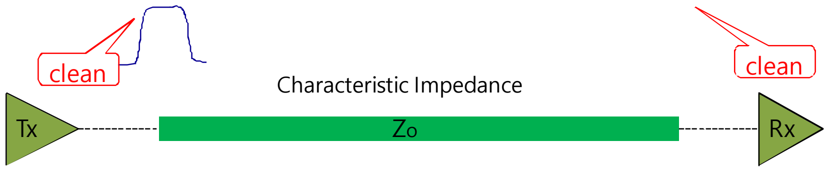
Coupled Microstrip

Coaxial Cable



Twisted Pair Cable

Ideal Transmission Line



No Reflection!

No Loss!

No Crosstalk!

No Mode conversion!

What is the Impedance?

Impedance

Impedance is represented as a complex quantity Z and the term *complex impedance* may be used interchangeably; the polar form conveniently captures both magnitude and phase characteristics,

$$Z = |Z|e^{j\arg(Z)}$$

where the magnitude $|Z|$ represents the ratio of the voltage difference amplitude to the current amplitude, while the argument $\arg(Z)$ (commonly given the symbol θ) gives the phase difference between voltage and current. j is the imaginary unit, and is used instead of i in this context to avoid confusion with the symbol for electric current. In Cartesian form,

$$Z = R + jX$$

where the real part of impedance is the resistance R and the imaginary part is the

Where it is required to add or subtract impedances the cartesian form is more co

form is used. A circuit calculation, such as finding the total impedance of two impe

Conversion between the forms follows the normal conversion rules of complex nu

The impedance of an ideal resistor is purely real and is referred to as a *resis*

$$Z_R = R.$$

In this case, the voltage and current waveforms are proportional and in phas

Ideal inductors and capacitors have a purely imaginary *reactive impedance*:

$$Z_L = j\omega L,$$

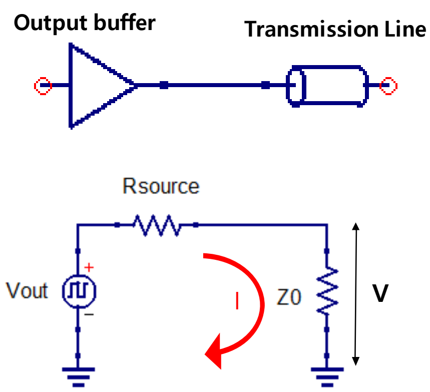
the impedance of inductors increases as frequency increases;

$$Z_C = \frac{1}{j\omega C},$$

the impedance of capacitors decreases as frequency increases.

<source: Wikipedia>

Input Impedance of Transmission Line



$$Z_0 = \frac{V}{I}$$

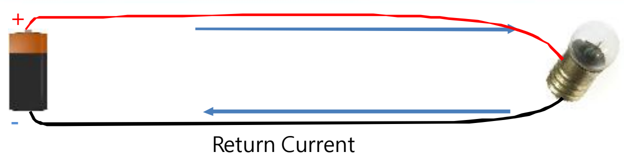
$$V = Vout \frac{Z_0}{Z_0 + Rsource}$$

Z_0 : Input Impedance of Tline

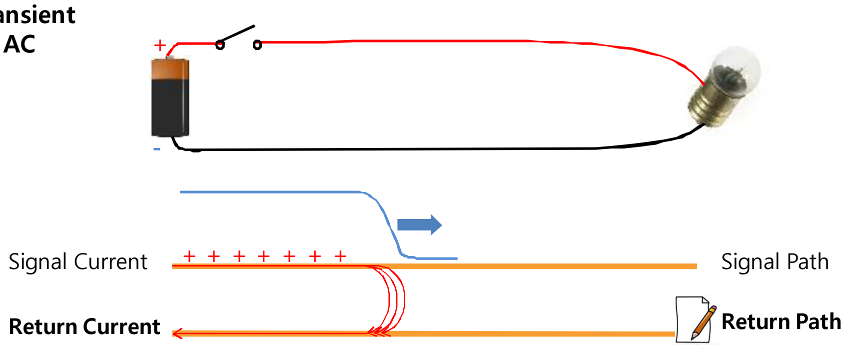
Characteristic Impedance of Tline

Current Flow in the Circuit

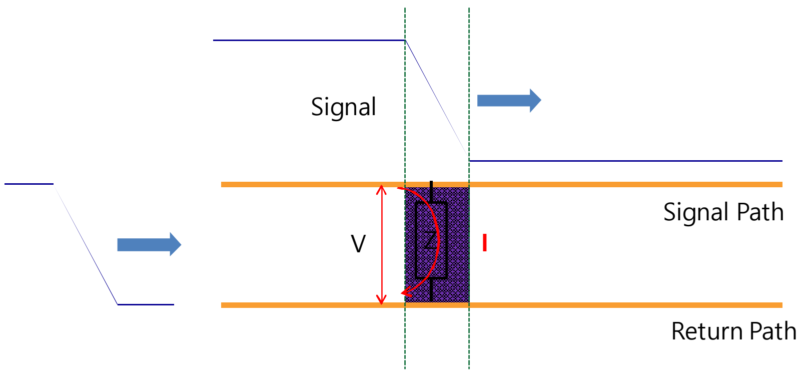
DC



Transient or AC



Instantaneous Impedance



ΔV/ Δt
ΔI / Δt

$$Z = \frac{V}{I}$$

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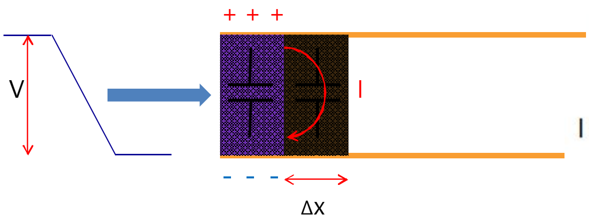
Impedance of a Transmission Line

$$Z = \frac{V}{I}$$

$$I = \frac{\Delta Q}{\Delta t} \qquad C = C_L \Delta x$$

$$\Delta Q = CV \qquad \Delta t = \frac{\Delta x}{v}$$



$$I = \frac{\Delta Q}{\Delta t} = \frac{vC_L \Delta x V}{\Delta x} = vC_L V$$

$$Z = \frac{V}{I} = \frac{V}{vC_L V} = \frac{1}{vC_L}$$

Q: charge, V: Voltage of the signal, I: current from the signal
C: capacitance
v: speed of signal in the material

Equation from <Eric Bogatin, Signal and Power Integrity>

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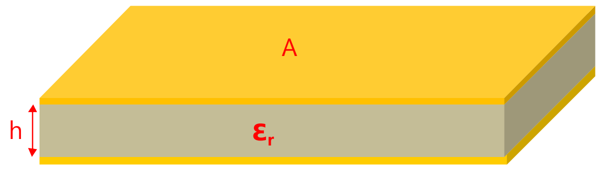
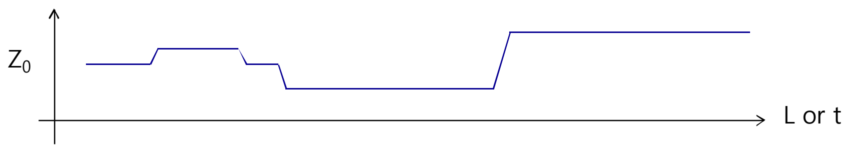
Capacitance

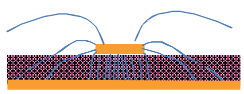


$$C = \varepsilon_0 \varepsilon_r \frac{A}{h}$$

C: capacitance of the plane, in pF
ε_0: permittivity of free space, 0.089pF/cm or 0.225pF/inch
ε_r: relative dielectric constant, typically ~ 4 in FR4
A: area of the plane, in inches
h: distance between the planes, in inches

Change of Instantaneous Impedance



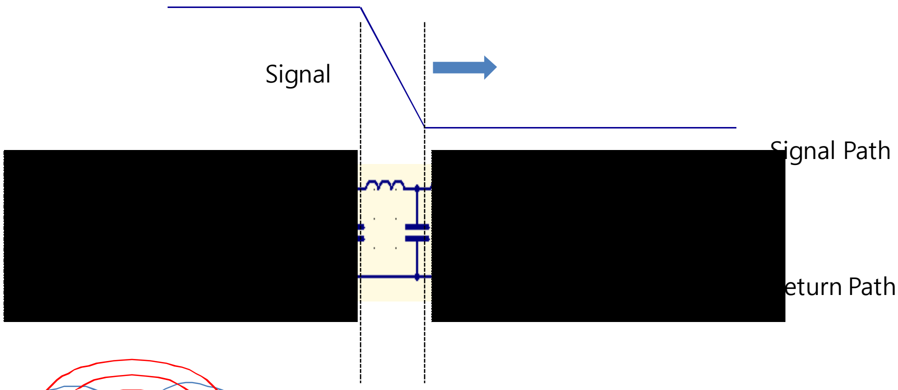


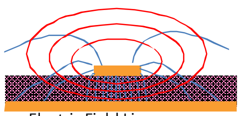
Electric Field Lines

$$Z_0 = \frac{1}{v\,C_L} = \frac{83}{C_L}\sqrt{\varepsilon_r}$$

v: the speed of light in the material
ε_r: dielectric constant of the material

Model of Transmission Line, LC





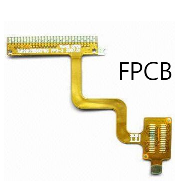
$$Z_0 = \sqrt{\frac{L_L}{C_L}}$$

* In modeling,
N section= 10 x BW(GHz) x Td(ns)

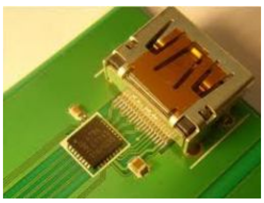
Characteristic Impedance, Z_0

Coax Cable

FFC



FPCB



PCB

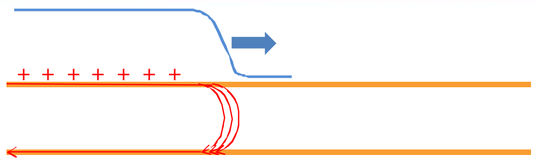
Uniform Transmission Line

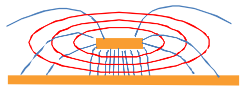
$$Z_0 = \sqrt{\frac{L_L}{C_L}}$$

Instantaneous Impedance is same through the Uniform Transmission Line
→ **Controlled Impedance**

✓**Characteristic Impedance** is **One Number** representing the Impedance of Transmission Line

Speed of Signal





Electric Field Lines
Magnetic Field Lines in Microstrip

$$v = \frac{1}{\sqrt{\varepsilon_0 \varepsilon_r \mu_0 \mu_r}}$$

v= speed of signal
ε_0 = permittivity of free space=8.89x10^{-12}F/m
εr =relative dielectric constant of the material
μ_0 =permeability of free space=4π x10^{-17}H/m
μ_r =relative permeability of the material

✓ In air,

$$v = \frac{2.99\times10^{8}}{\sqrt{\varepsilon_r \mu_r}} \frac{m}{secs} = \frac{11.9}{\sqrt{\varepsilon_r \mu_r}} \frac{inches}{nsecs}$$

✓In FR4, μ_r is 1, ε_r is 4 $\quad v = \frac{11.9}{\sqrt{4}} \frac{inches}{nsecs}$

approximation

6inch / 1ns (@FR-4 PCB)

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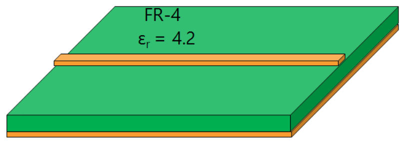
Propagation Velocity, Time Delay

$$v = \frac{C}{\sqrt{\varepsilon_r}}$$

$$PD = \frac{1}{v} = \frac{\sqrt{\varepsilon_r}}{C}$$

$$TD = \frac{x\sqrt{\varepsilon_r}}{C}$$



$$TD = \sqrt{L\,C}$$

- v=propagation velocity, in meters/sec
- C = speed of light in a vacuum (3x10^8m/s)
- ε_r = dielectric constant
- PD= propagation delay, in seconds per meter
- TD = time delay for a signal to propagate down a transmission line of length x
- x = length of transmission line, in meters

L= total series inductance for the length of the line
C= total shunt capacitance for the length of the line

✓Higher Dielectric constant, Inductance, Capacitance make signal slower in Tline.

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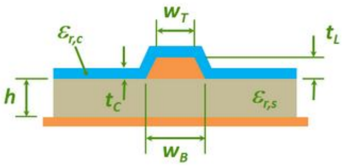
Transmission Line Impedance Calculator

Coated Microstrip



Top width (w_T):	355	μm
Bottom width (w_B):	365	μm
Substrate height (h):	200	μm
Thickness (t):	17	μm
Coating thickness (t_C):	13	μm
Dielectric constant ($\varepsilon_{r,1}$):	4.3	
Dielectric constant ($\varepsilon_{r,2}$):	3.3	

Results

Z0	49.8 Ohm
ErEff	3.3
Cs	121.7 pF/m
Ls	301.9 nH/m
Velocity	164898416 m/s
PropDelay	6.064 ns/m

<Calculated by STLC (Sequid Transmission-Line Online-Calculator)>

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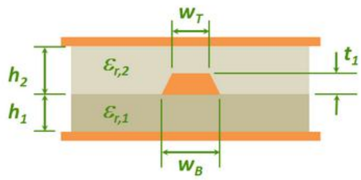
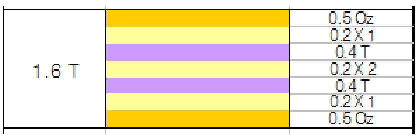
Transmission Line Impedance Calculator

Stripline





Top width (w_T):	210	μm
Bottom width (w_B):	220	μm
Substrate height (h_1):	200	μm
Substrate height (h_2):	400	μm
Thickness (t):	17	μm
Dielectric constant ($\varepsilon_{r,1}$):	4.3	
Dielectric constant ($\varepsilon_{r,2}$):	4.3	

Results

Z0	50.1 Ohm
ErEff	4.3
Cs	137.9 pF/m
Ls	346.5 nH/m
Velocity	144572720 m/s
PropDelay	6.917 ns/m

<Calculated by STLC (Sequid Transmission-Line Online-Calculator)>

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Dielectric Constant

ε_r : Dielectric Constant

Relative Permittivity, Dk

the property of the insulating material between the conductors.

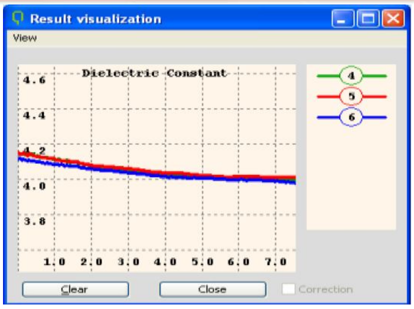
increase the capacitance of conductors.

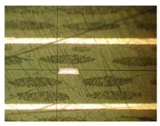
$$\varepsilon_r = \frac{C}{C_0}$$

Material	ε_r
Air	1
Teflon	2.1
PTFE	2.8
FR4	4-4.7
Nelco	3.36
Rogers	3.5
Water	8

ε_r = relative dielectric constant of the material
C = capacitance when conductors are in the material
C0 = capacitance when conductors are in the air

Dielectric Constant of FR4 over Frequency





<Microsection of Stripline>

<Example of Measured Dielectric constant vs Freqeuncy
From 10MHz to >5GHz, source: Sequid GmbH>

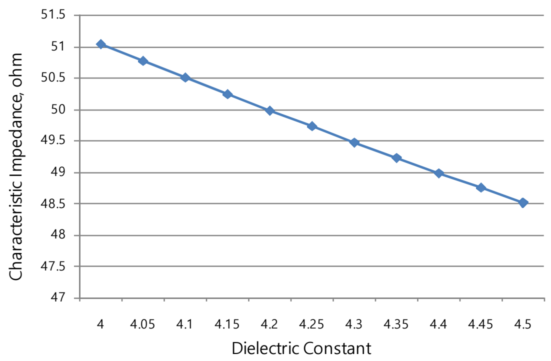
✓The dielectric constant of FR4 is sometimes vary with frequency, especially below 10MHz.

✓In higher frequency it will be more constant.

✓Real value of Dielectric Constant of FR4 varies depending on the relative amount of epoxy resin and glass weave.

✓The variation of dielectric constant of FR4 during production may be bigger than frequency variation.

Dk and Characteristic Impedance



Variation of dielectric constant from 4.0 to 4.5
can make impedance variation from 51ohm to 48.5ohm in FR4 PCB.
Calculated with QUCS line calculator.

Choice of Characteristic Impedance?

Attenuation in Coax cable ≒ Series Resistance of inner, outer conductors / Z_0

✓30, 60, 77ohm were determined at Bell Lab. In 1929 for high power, high voltage, low attenuation.

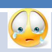
RG59: 75ohm Coax Cable → CATV. Low-attenuation is important. Easy to make 4:1 balun transformer to be used with 300ohm anntena.

TV antenna: 300ohm → Close to the Impedance of free space, 377ohm. Optimized for radiating energy.

RG62: 93ohm Coax Cable → Computer network in 1970 and early 1980s. Low Capacitance per unit-length is important for Square wave

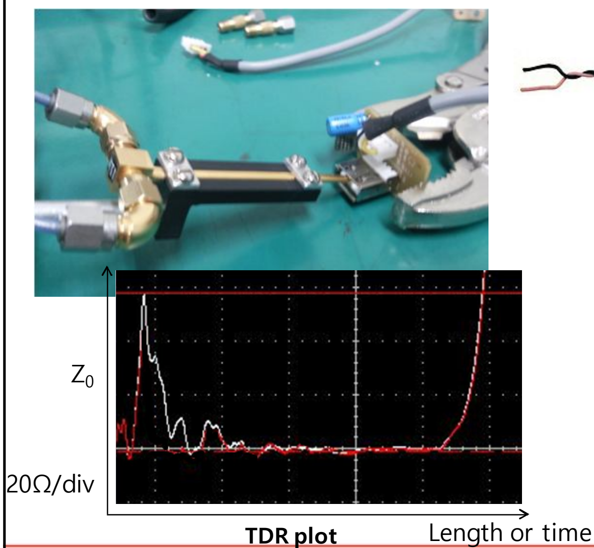
✓50ohm is a compromise between power handling and attenuation. Commonly used in many of transmission lines.

Value of Z_0 and Trade-offs in Digital System

	Lower Z_0	Higher Z_0
Board Costs		
Delay Adder		
Cross Talk		
Attenuation		
Connector Costs		
Twisted pair/cable costs		
Driver Design		
Power dissipation		

✓ **50ohm** is good starting points among trade-offs.

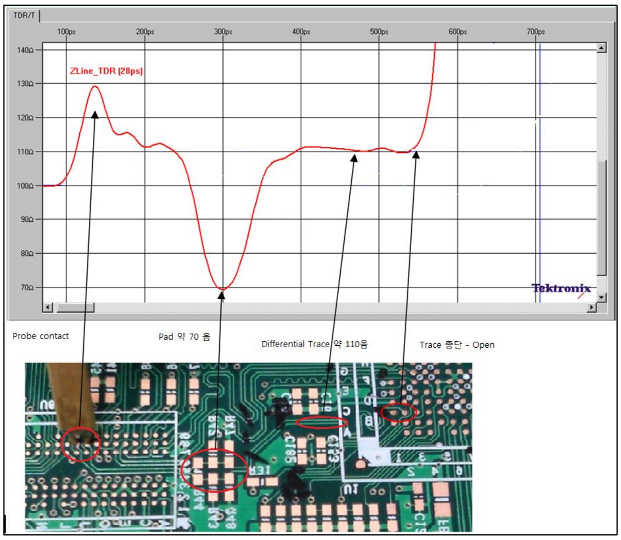
Inductive High Impedance



Inductive Discontinuities

- Connectors
- Joint of cable assembly
- Slit of Ground(Return) plane
- Differential Trace near Pads
- Vias
- etc.

Capacitive Low Impedance



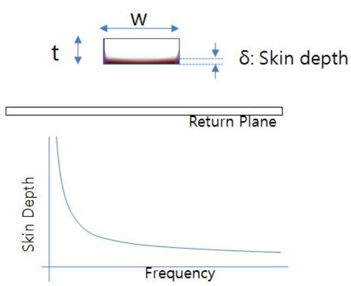
Capacitive Discontinuities

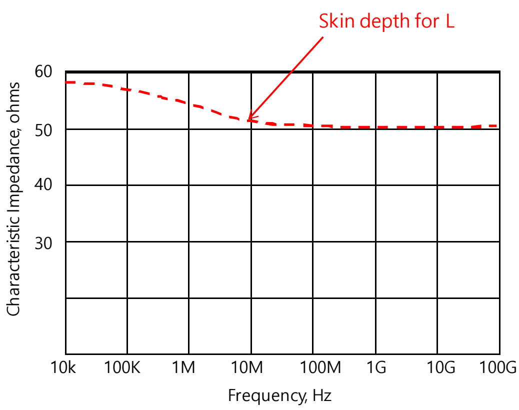
- Decoupling capacitor Pads
- Termination resistor Pads
- Filter Pads
- Connector and Pads
- Stubs
- Vias
- etc.

Characteristic Impedance vs Frequency

✓ lossless TL (when Dielectric constant is constant)

$$Z_0 = \sqrt{\frac{L_L}{C_L}}$$





Typical PCB characteristic Impedance with Frequency

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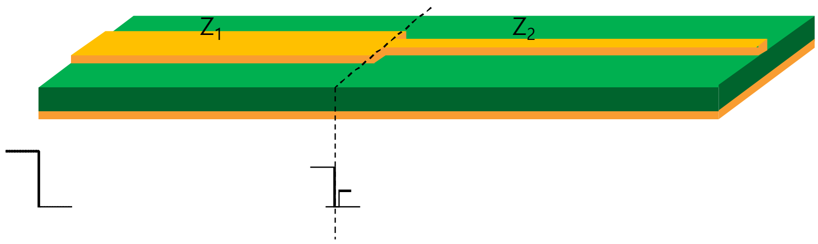
Reflection
Termination topology
Discontinuity

Reflections at Impedance changes



$$\frac{V_{reflected}}{V_{incident}} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \rho$$ (Rho; 반사계수)

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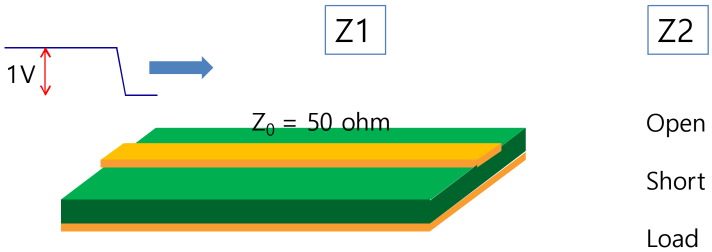
Reflections at the End of the Line - Termination



- Open
- Short
- Load
  - Matched
  - Unmatched

$$\frac{V_{reflected}}{V_{incident}} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \rho$$

(Rho; 반사계수)

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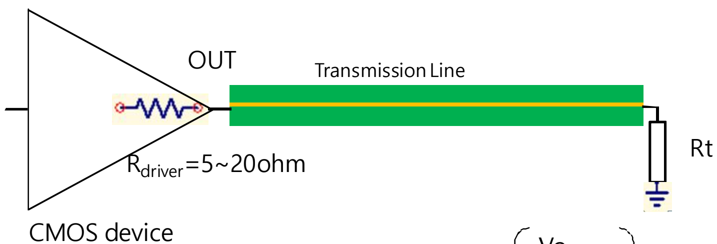
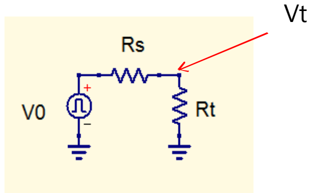
Source Impedance of Device Output



R_{driver} = Rs



$$Rs = Rt\left(\frac{Vo}{Vt} - 1\right)$$

Ex) Vo=3.3V, Rt=10ohm, Vt=1.9V → Rs≒7.3ohm

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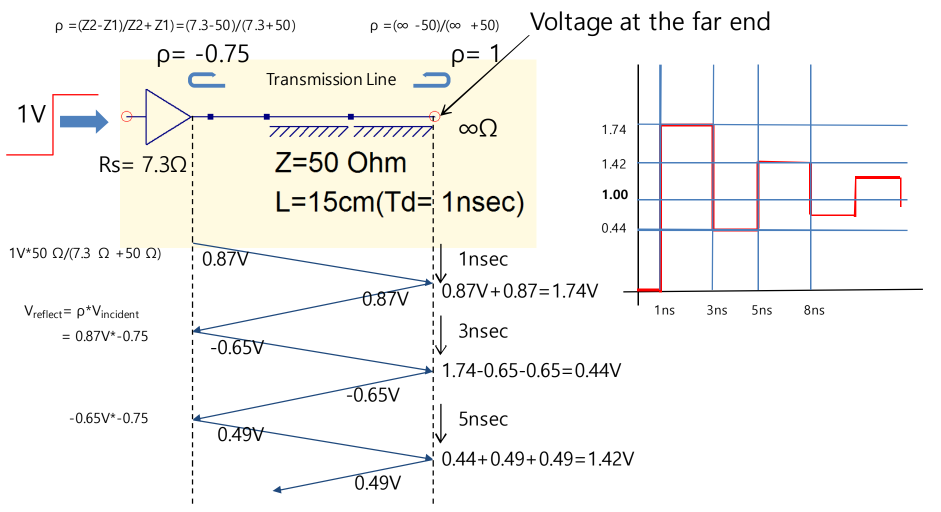
Bounce Diagram



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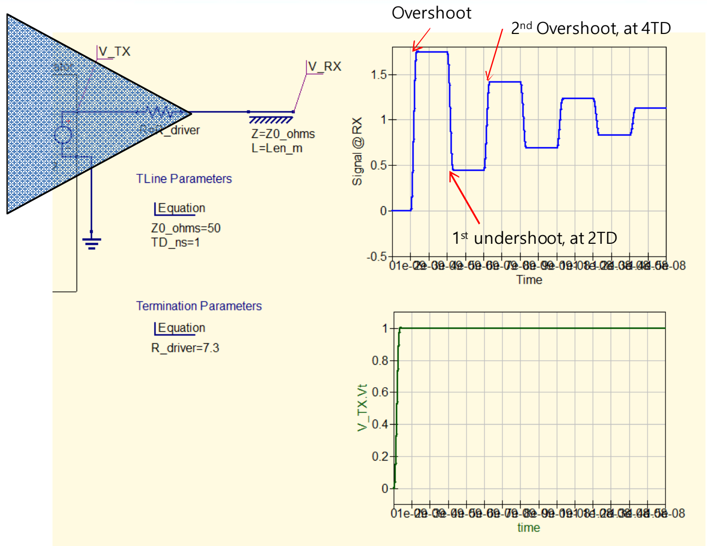
Bounce Simulation



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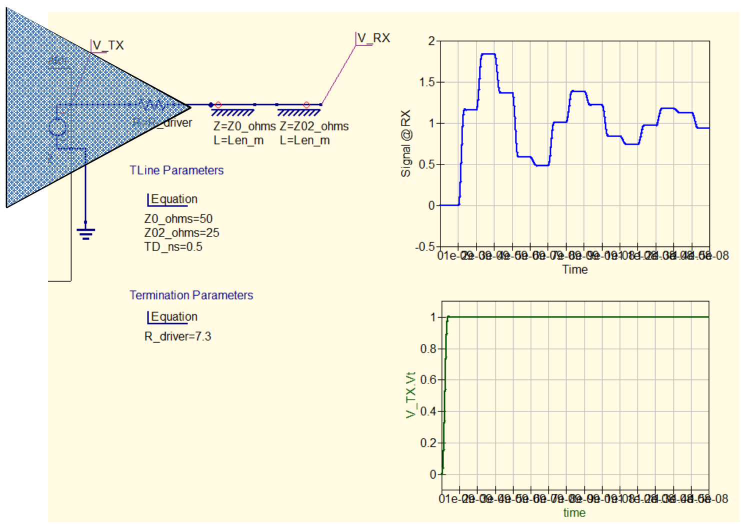
Bounce Simulation_Multi Reflection



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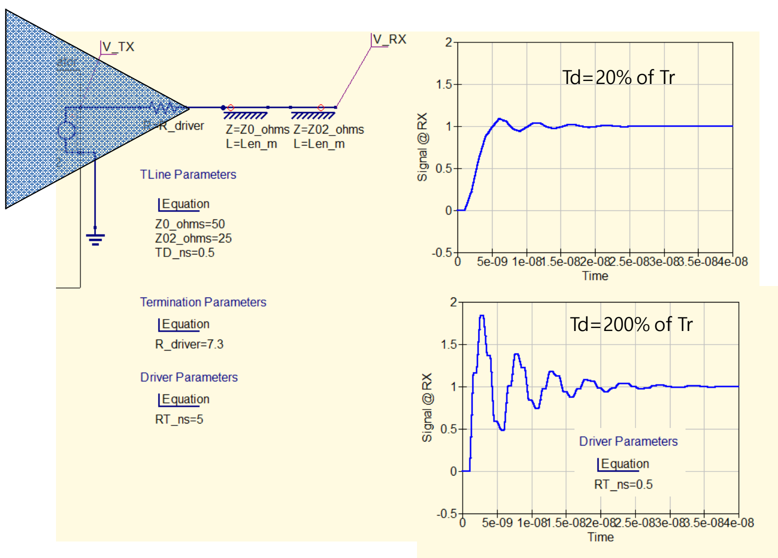
Reflection of T.line and Rise Tme



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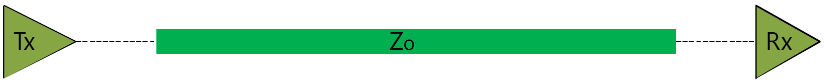
Termination

Match Impedance to eliminate Reflection at Source or(and) Far-end.



Source Series Termination

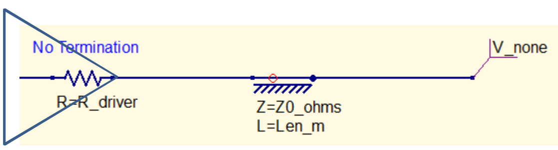
Far-end Parallel Termination

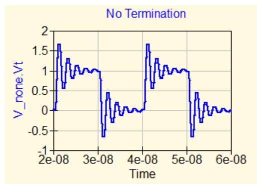
Far-end RC Termination

Far-end Thevenin Termination

Vtt Termination

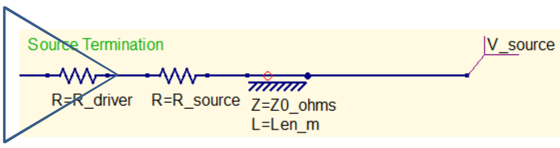
Source Series Termination

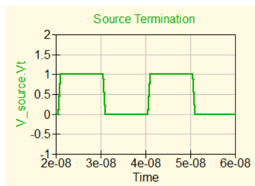




Driver
Driver Impedance=10ohm
Tr=0.5ns
V=1V

Transmission Line
Z_0=50ohm
Td=0.5ns

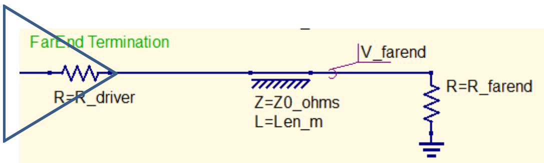


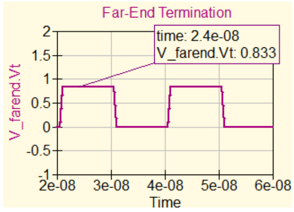


Source Series Termination Resistor
R_driver+R_source=Z_0=50ohm

✓Low current consuming
✓Only for point to point topology

Far-end Parallel Termination





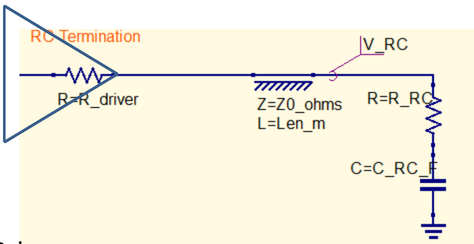
Driver
Driver Impedance=10ohm
Tr=0.5ns
V=1V

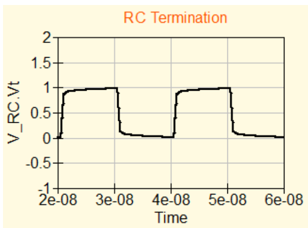
Transmission Line
Z_0=50ohm
Td=0.5ns

Far-end Termination Resistor
R_farend=Z_0=50ohm

✓Eliminate the unknown variable of buffer Impedance
✓Large DC current consuming during state "1" at the load
✓Voltage is divided by R_{driver} and R_{farend}

Far-end RC Termination





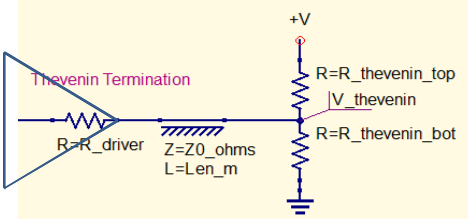
Driver
Driver Impedance=10ohm
Tr=0.5ns
V=1V

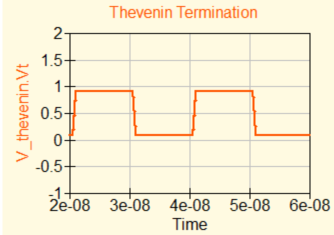
Transmission Line
Z_0=50ohm
Td=0.5ns

Far-end Termination
R_RC=Z_0=50ohm
C_RC→ chose such that RC time constant is appx equal to one or two rise time.
2.2RC ~ T_{rise}
Simulation is needed to chose exact C value

✓As charging the capacitance, the DC power dissipation will be reduced.
✓Capacitive Loading will increase the signal delay by slowing down the rise time
✓Board space and cost

Far-end Thevenin Termination





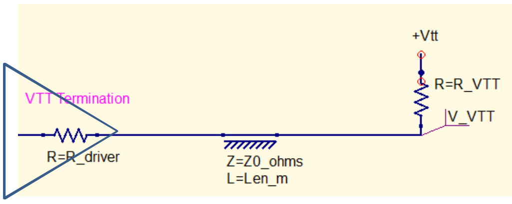
Driver
Driver Impedance=10ohm
Tr=0.5ns
V=1V

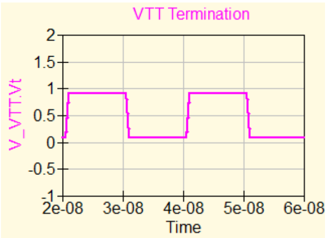
Transmission Line
Z_0=50ohm
Td=0.5ns

Far-end Termination
Parrallel combination of R_top and R_bot=Z_0=50ohm

✓Pull-up and Pull-down R help stable logic state thereby improve the noise margin
✓Smooth power dissipation variation helps signal integrity
✓Constant flow of DC current from V+ to Gnd, high power dissipation
✓Board space and cost

Vtt Termination





Driver
Driver Impedance=10ohm
Tr=0.5ns
V=1V

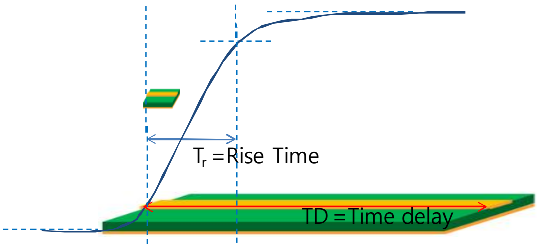
Transmission Line
Z_0=50ohm
Td=0.5ns

Vtt Termination
R_vtt=Z_0

✓Behave like as pull-up makes stable logic state
✓Improving signal integrity because of constant load current
✓Less power dissipation over the Thelevin termination

When should we terminate the line?

✓ **Time delay vs Rise Time**



Termination is required for
Td > 20% of Rise Time

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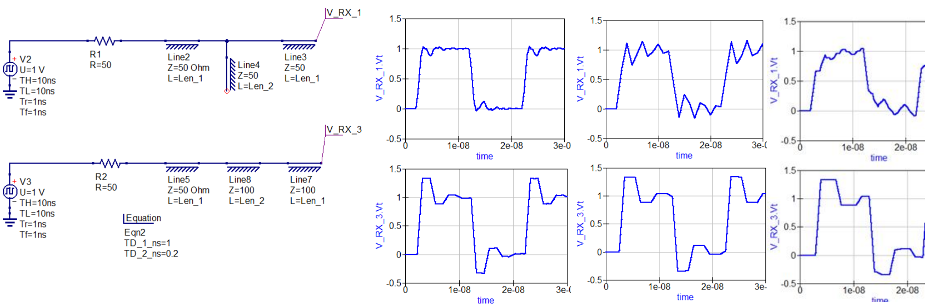
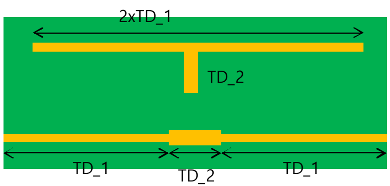
Length of Impedance Discontinuity



TD=20% of Tr

TD=50% of Tr

TD=110% of Tr



Stub and Series discontinuities

TD of discontinuities should be,
TD_{disc} < 20% of Rise Time

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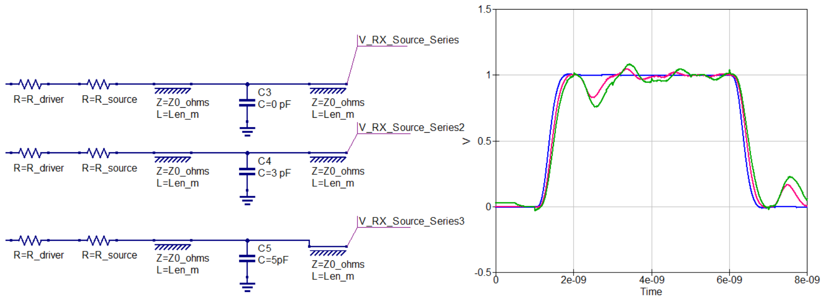
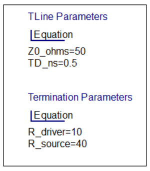
Capacitive Discontinuity with Series Termination

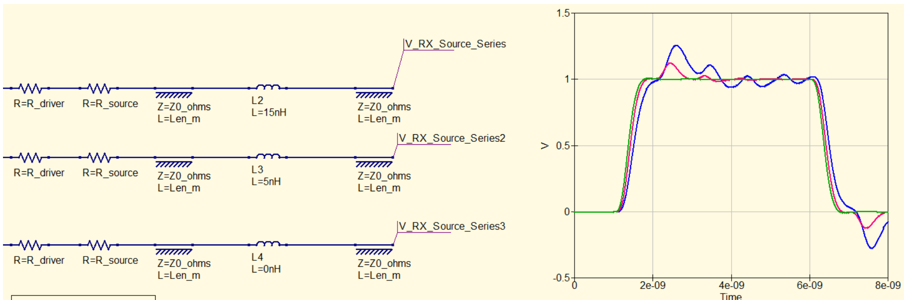


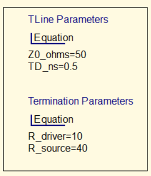
Tr=0.2ns



Capacitance: via, component pads, connector, stub, test pads.
Makes discontinuity and delay adder.

Inductive discontinuity with Series Termination



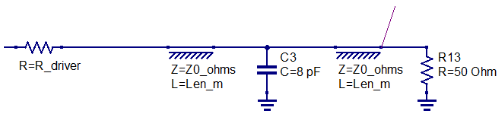


Green: 0nH
Red: 5nH
Blue: 15nH

Series Inductance: via, series resistor, connector, wire, etc.
Makes discontinuity and delay adder.

Tr=0.2ns

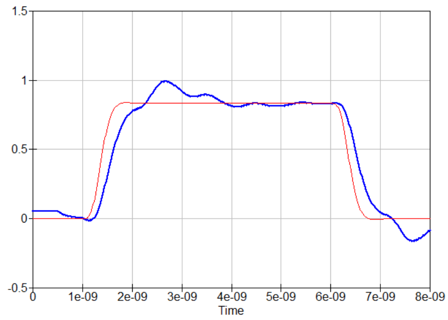
Capacitive discontinuity with Far-end Termination



Tr=0.2ns

TLine Parameters
Equation
Z0_ohms=50
TD_ns=0.5

Termination Parameters
Equation
R_driver=10



Red: without C Stub
Blue: with 8pF C Stub

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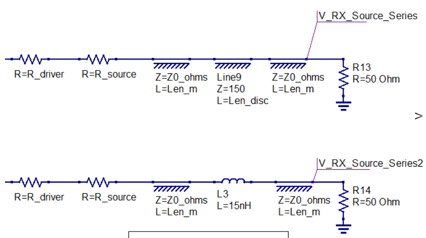
Inductive discontinuity with Far-end Termination

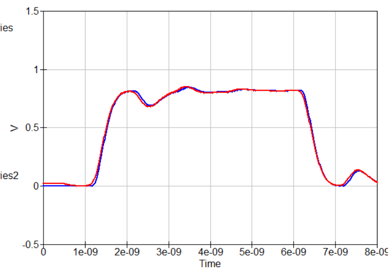


Tr=0.2ns

TLine Parameters
Equation
Z0_ohms=50
TD_ns=0.5

Termination Parameters
Equation
R_driver=10
R_source=1

Equation
Len_disc_ns=0.1



Red: Z=150ohm, Td 0.1ns
Blue: 15nH Inductance

15nH ~ Td 0.1ns ,150ohm disc.

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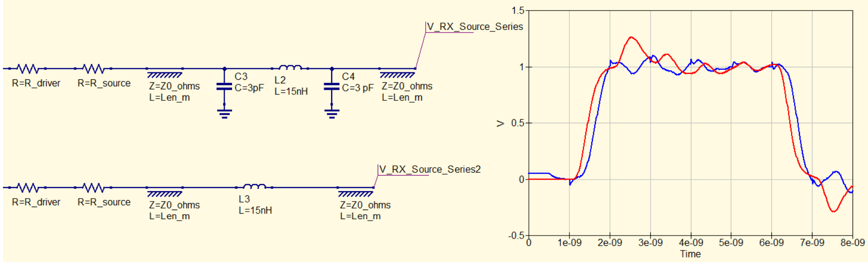
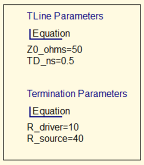
Compensation of Inductive discontinuity



Red: before compensation
Blue: after compensation

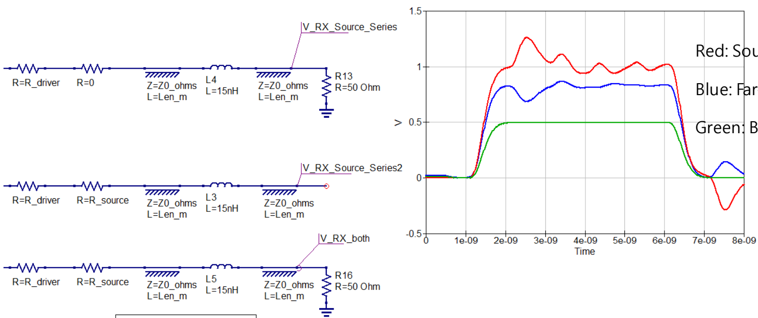
Tr=0.2ns



$$Z_0 = \sqrt{\frac{L_L}{C_L}}$$

$$C = L / Z_0^2$$

Discontinuity and Termination Topologies

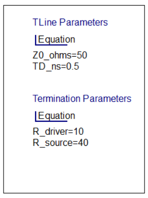


Red: Source Term.

Blue: Far-end Term.

Green: Both end Term.

Tr=0.2ns



✓Both end termination eliminate reflections, but amplitude will be reduced to half.

Time Delay by Impedance discontinuity-C, L

✓ **Delay adder**

Capacitive

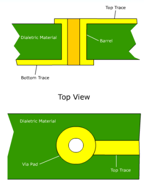
$\Delta Td \approx 0.5\ Z_0 C$

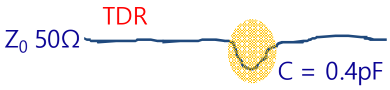
Inductive

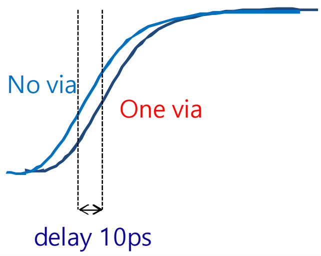
$\Delta\ Td \approx 0.5 \frac{L}{Z_0}$

Ex)

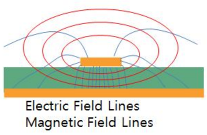
$\Delta\ Tdd = 0.5 \times 50 \times 0.4E\text{-}12 = 10ps$



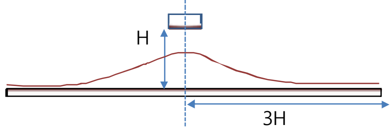


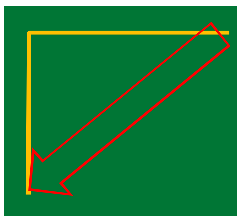


Return Path

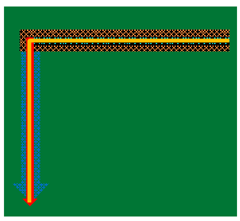


Current density distribution in the return plane

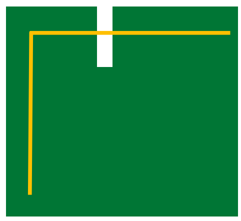




Return current flow at DC



Return current flow at high frequency



Slit on return plane

✓ In high speed frequency, solid return path is important as much as signal line.

Impedance discontinuity

The End of the line

Corner

Connector

Stub

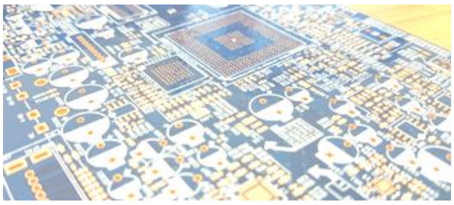
Test Pad

Package Lead

Branch

Via

Gap in the return path

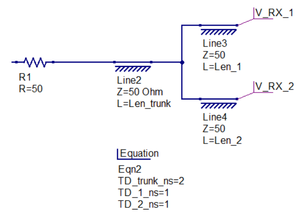


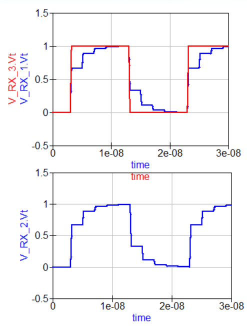
Pad for Components

Input Gate Capacitance

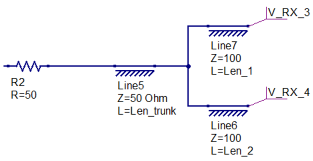
Topology

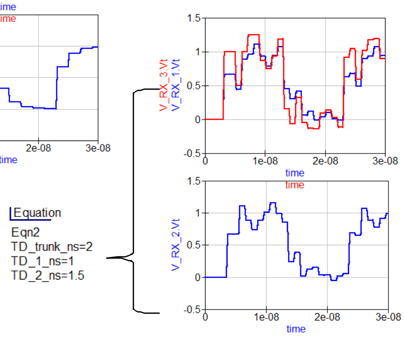
✓Balanced length of branches





✓Unbalanced length of branches

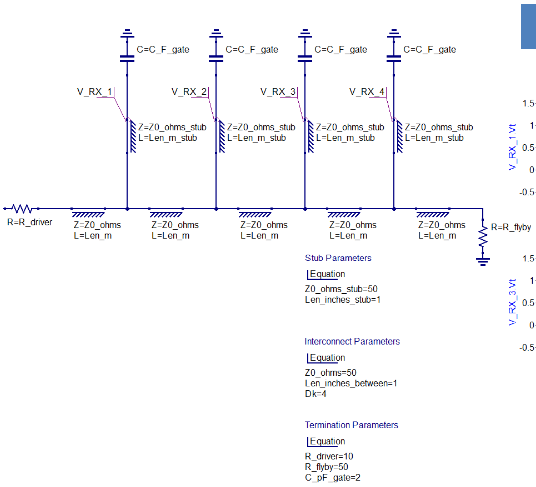


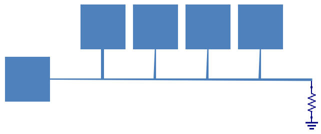


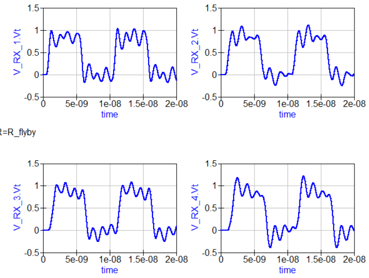
✓Topology must looks symmetric from the point of view of any driving agent.
✓Impedance, Length and loading of each leg.

Daisy chain topology

Daisy chain: multi drop buses

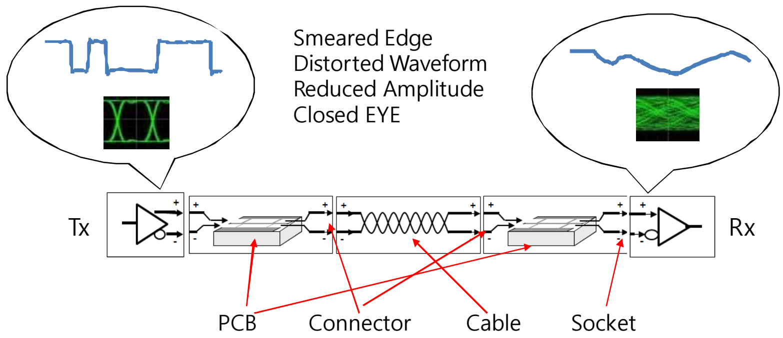






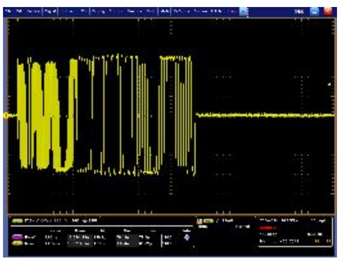
Signal Loss
S-parameters
Loss compensation

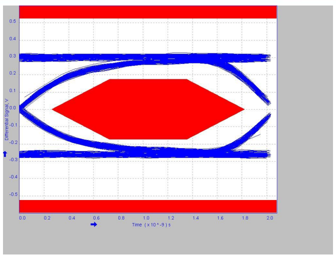
Loss of Transmission Line



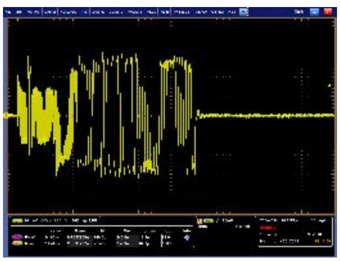
✓ Loss influences more on the closed EYE in Gpbs.

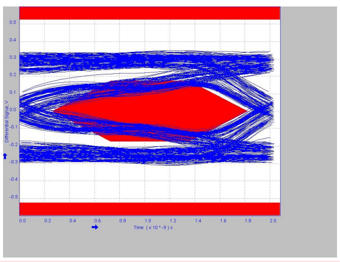
Example of Loss: Waveform and EYE diagram





Frequency dependant Loss!





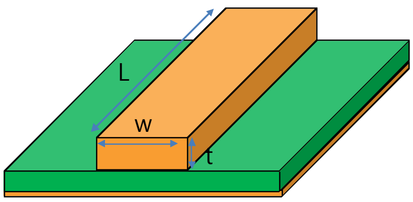
5 sources of Energy Losses in Tline

- Radiative Loss
- Coupling to adjacent Traces
- Impedance mismatches
- Conductor loss
- Dielectric Loss

Small ↑ ↓ Big

Source of Loss: DC Loss

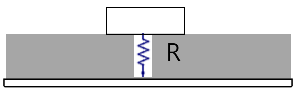
Conductor DC Loss



$$R = \rho \frac{L}{wt}$$

R: Resistance of conductor, in ohm
ρ: Bulk resistivity of conductor, in ohm/inch
L: Length of the line, in inch
w: Conductor width, in inch
t: conductor thickness, in inch

Dielectric DC Loss

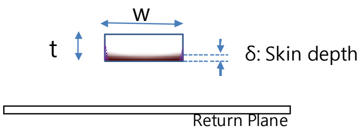


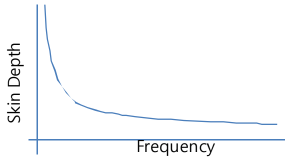
R @ DC is very high(eg. 10^{12}ohm-cm)

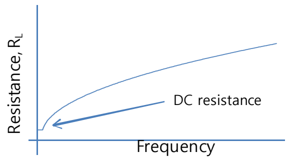
Dielectric DC loss is negligible and can be ignored.

Source of Loss: AC Loss

Conductor AC Loss







$$R = \rho \frac{L}{w\delta}$$

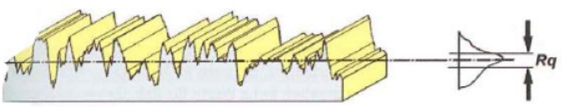
R: Resistance of conductor, in ohm
ρ: Bulk resistivity of conductor, in ohm/inch
L: Length of the line, in inch
w: Conductor width, in inch
t: Conductor thickness, in inch
δ: Skin depth, in inch

$$\delta = \sqrt{\frac{\rho}{\pi F \mu}}$$

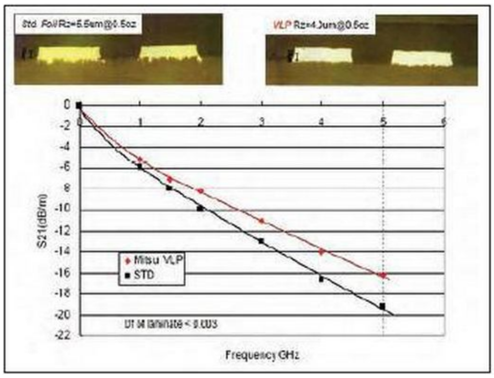
δ: Skin depth
ρ: Bulk resistivity of conductor
F: frequency
μ: permeability of free space

$$R_L = R_{DC} + R_{AC}\sqrt{F}$$

Source of Loss: Surface Roughness



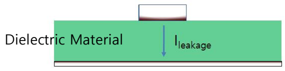
✓Skin effect and surface roughness increase AC resistance.

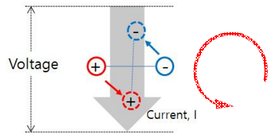


Ex) 3dB difference in S21 at 5GHz between Std foil and VLP foil.
(Courtesy of Oak-Mitsui)

Source of Loss: AC Loss

Dielectric AC Loss





<Electric Polarization; dipole movement >

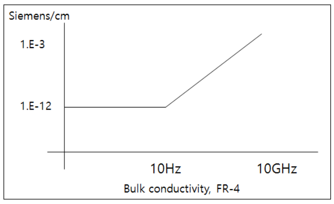
- ✓ When voltage is applied across capacitor
- ✓ Electric Field is generated
- ✓ Dipole of the material will tend to align in the direction of field
- ✓ Dipoles motion generates the leakage current
- ✓Current heat the material and dissipate the energy

✓Faster AC voltage makes faster movement of dipoles and higher current

Higher the Frequency, higher the leakage conductivity, and the higher the power dissipation in the dielectric

Rise time degradation

Conductance, G= 1 / R



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Dissipation Factor of the material

✓As frequency increase, the conductivity of the material increase due to the motion of the dipole.

✓The more dipoles, the farther dipoles move make the higher conductivity.

Dissipation factor of the material

tan(δ), Df

measure of the number and how far each of them can rotate

$$\tan(\delta) \backsim n \times p \times \theta_{max}$$

n: the number of density of dipoles in the dielectric
P: the dipole moment, a measure of charge and separation of each charge
θ_{max}: how far the dipoles rotate in the applied field

✓ In the real, Df at high frequency can be changed nonlinearly due to the variation of θ_{max}.

The bulk conductivity of the dielectric

$$\sigma = 2\pi f \times \varepsilon_0 \varepsilon_r \times \tan(\delta)$$

Material	ε_r	tan(δ)
FR-4	4.0~4.7	0.02
GETEK	3.5	0.009
Nelco N9000	3.0~3.5	0.004
Rogers RO3003	3.0	0.0013
DiClad880	2.2	0.0009

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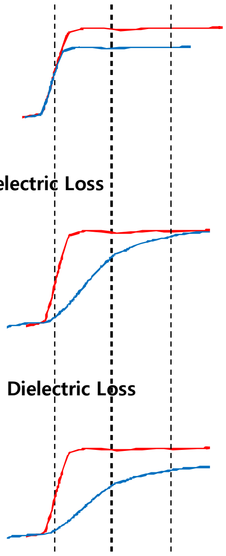
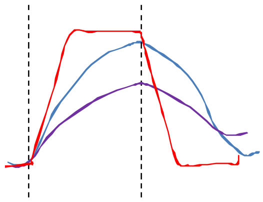
Time domain Waveforms with source of Loss

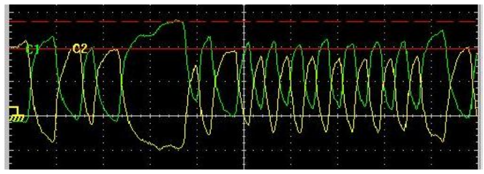
DC conductor Loss

AC conductor Loss + Dielectric Loss

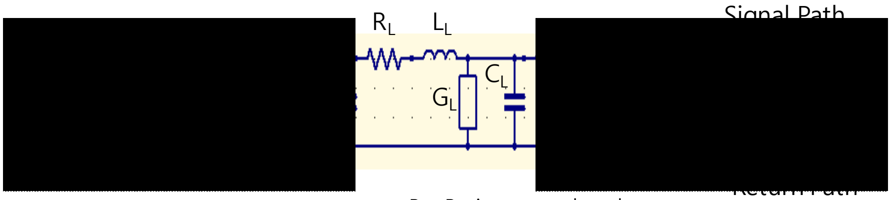
DC AC conductor Loss + Dielectric Loss







Model of Lossy Transmission Line, RLGC



[redacted]

$G_L = 1 / R_{leakage}$

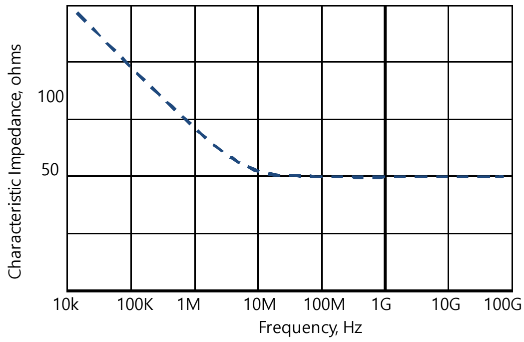
R_L = Resistance per length
L_L = Inductance per length
G_L = Conductance per length
C_L = Capacitance per length

$$Z_0 = \sqrt{\frac{R_L + \omega L_L}{G_L + \omega C_L}}$$

Characteristic Impedance with Loss

$$Z_0 = \sqrt{\frac{R_L + \omega L_L}{G_L + \omega C_L}}$$

✓Above 2MHz on 3mil trace, the impedance of resistance is much smaller than the reactance of the inductance.
✓The conductivity is much smaller than the reactance of the capacitance when tan(δ) ≪1.
0.02 in FR4 and <0.001 in some low loss materials.



3mil wide 50ohm Microstrip, FR-4

Signal Velocity with Loss

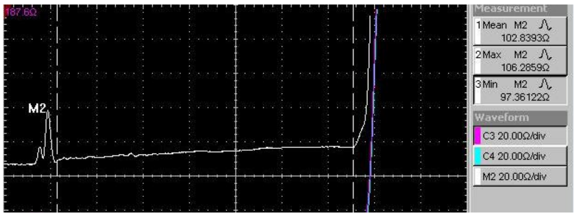
$$v = \frac{\omega}{\sqrt{\frac{1}{2}\left[\sqrt{(R_L^2+\omega^2 L_L^2)(G_L^2+\omega^2 C_L^2)} + \omega^2 L_L C_L - R_L G_L\right]}}$$

✓ When the impedance of resistance is much smaller than the reactance of the inductance.
✓ When the conductivity is much smaller than the reactance of the capacitance when tan(δ) ≪1.
0.02 in FR4 and <0.001 in some materials.

$$v = \frac{1}{\sqrt{L_L C_L}}$$

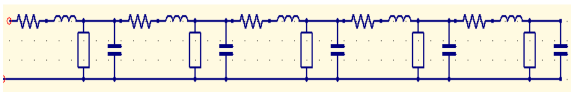
✓ Above 10MHz, for 3mil FR4 50ohm microstrip, Signal speed is **not affected by the loss**.

TDR waveform with Loss

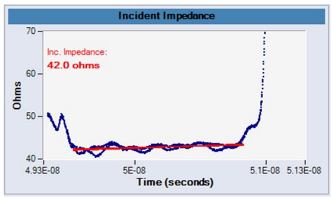


TDR waveform of Uniform Transmission Line with dribble up effect

Model of Lossy Transmission Line



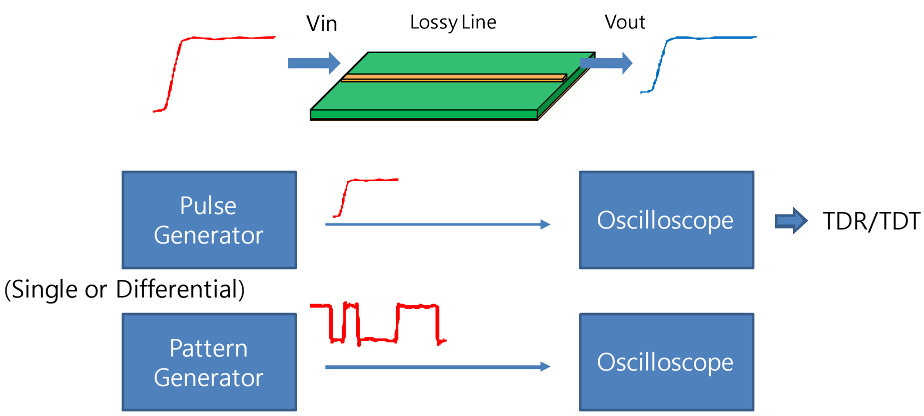
Incident Impedance



<Source: Introbotix>

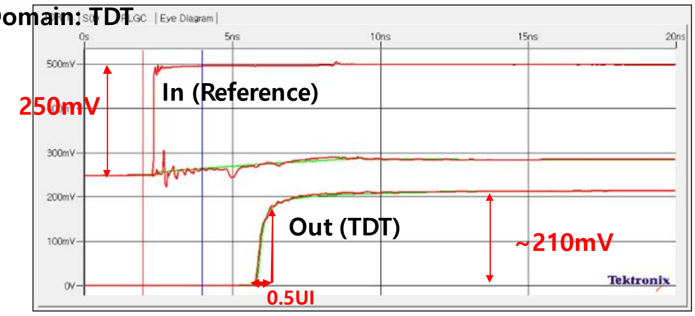
Measured Example of Lossy Transmission Line

Time Domain: TDT(Time Domain Transmission), or Pulse Response Test



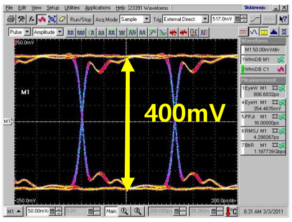
Measured Example of Lossy Transmission Line

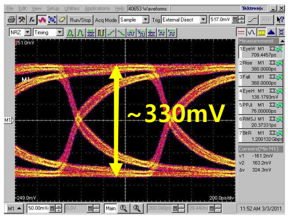
Time Domain: TDT



EYE measurement @1.2Gbps, 400mV

In

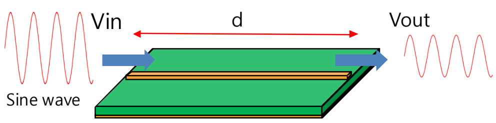




Out

Loss in Frequency domain

Attenuation



$$V_{out} = V_{in}exp(-A_n) = V_{in}exp(-d \times \alpha_n)$$

V_{out}= the voltage at the end of the line
d= the distance of the line, in inch
V_{in}= the amplitude of the input voltage
A_n =the total attenuation, in neper
α_n =the attenuation per length, in neper/inch

✓**The attenuation increases exponentially with distance.**

Loss in Frequency domain

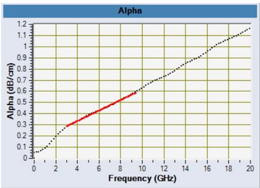
Attenuation in dB

$$V_{out} = V_{in}10^{-\frac{A_{dB}}{20}} = V_{in}10^{\left(-d \times \frac{\alpha_{dB}}{20}\right)}$$

A_{dB} =the total attenuation, in dB
α_{dB} =the attenuation per length, in dB/inch
20= the factor to convert dB into amplitude

$$Ratio(dB) = 10 \times \log \frac{P_1}{P_0} = 10 \times \log \left(\frac{V_1^2}{V_0^2}\right) = 20\log\left(\frac{V_1}{V_0}\right)$$

$$Ratio = \frac{V_1}{V_0} = 10^{\frac{ratio_{dB}}{20}}$$



<measured α_{dB} in FR4 PCB, in dB/cm>

dB	Power ratio	Voltage ratio
30	1000	100
20	100	10
10	10	3.16
6	4	2
3	2	1.4
0	1	1
-3	0.5	0.7
-6	0.25	0.5
-10	0.1	0.316
-20	0.01	0.1
-30	0.001	0.01

✓**In dB, the attenuation increases linearly with frequency.**

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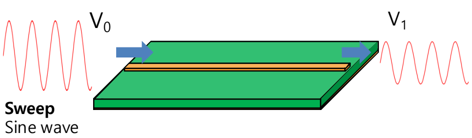
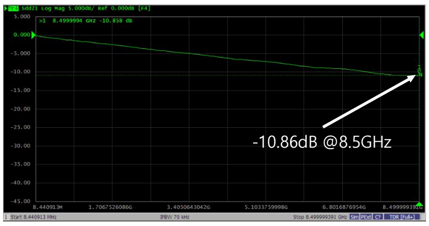
Loss in Frequency domain

Insertion Loss



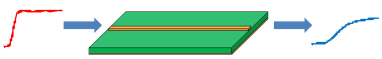


<Measured insertion loss in FR4 PCB, 20cm differential line. Measured with Agilent VNA 5071C.>

$$Ratio(dB) = 20\log\left(\frac{V_1}{V_0}\right)$$

✓Higher frequency is attenuated more than lower frequency.

➡ Rise time degradation at the end of lossy line



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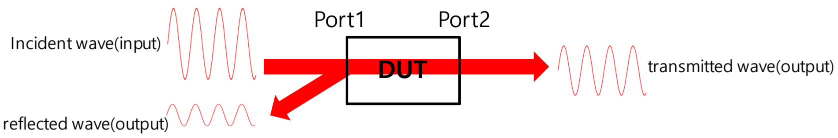
Loss in Frequency domain

S-parameters

"Scattering-parameters"
Origins in RF world, this technique has been widely used to describe the behavior of any interconnects in time domain in the digital world.



✓Incident wave scatter back into the source, reflected wave: **S11 or Return Loss**

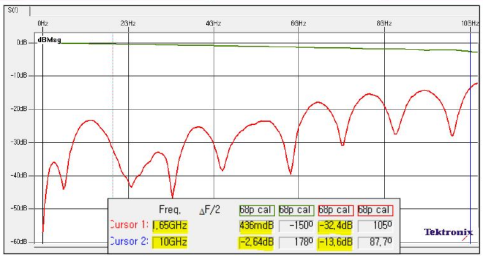
✓Incident wave scatter through the device, transmitted wave: **S21 or Insertion Loss**

$$\text{mag(S)} = \frac{\textbf{amplitude of output sine wave}}{\textbf{amplitude of input sine wave}}$$

$S_{dB} = 20\log(\text{mag(S)})$ **Phase(S)= Phase(output sine wave) – Phase(input sine wave)**

S-parameters

<50ohm Transmission line, FR4, 5cm>



<Measured S21 and S11 plot. Measured with Tektronix DSA8300/80E04. Calculated and displayed with I-Connect SW>

In all linear, passive devices, S21=S12. S11=S22.

S21(Insertion Loss) describes how big the transmitted signal will be, at each frequency.
Ex) 1V, 10GHz, sine wave will be reduced to 0.738V(-2.64dB) at the output port.
This Frequency is the appx. **Bandwidth(-3dB) of this device**.

$$\text{Ratio} = \frac{V_1}{V_0} = 10^{\frac{ratio_{dB}}{20}}$$

S11(Return Loss) describes how small the reflected signal will be, at each frequency.
Ex) 0.2V(-13.6dB) out of 1V, 10GHz, sine wave will be returned back to the source.

S21 and S11

The relationship between S21 and S11

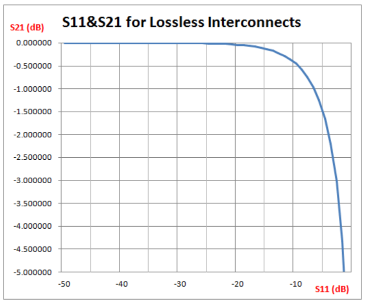
$$1 = S11^2 + S21^2$$

$$S21 = \sqrt{1 - S11^2}$$

Ex)

$$S11 = \frac{(75-50)}{(75+50)} \fallingdotseq 0.2 \fallingdotseq -14dB$$

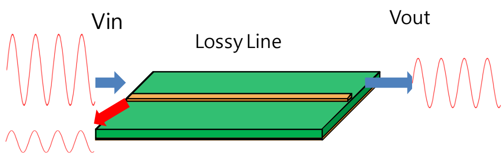
$$S21 = \sqrt{1 - 0.2^2} \fallingdotseq 0.98 \fallingdotseq -0.18dB$$



✓ -14dB(20%) reflection affects only -0.18dB(2%) on Insertion loss.
While more than 10dB loss in S11 will dramatically affect on insertion loss.

Measured Example of Lossy Transmission Line

Frequency Domain: Insertion Loss/Return Loss, or S21/S11



Vector Network Analyzer (VNA)

2 port(for Single-end)
4port(for Differential)

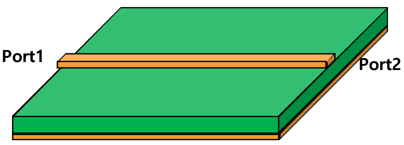
Signal Generator

Spectrum Analyzer

(S21 only)
(Scalar Network Analyzer)

S-parameters of Single & Differential T.line

Single-end Line

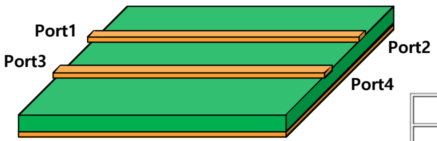


2Port S-parameters

S11 S12
S21 S22

➡ **Touchstone file: .S2P**

Differential Line



4Port S-parameters

S11 S12 S13 S14
S21 S22 S23 S24
S31 S32 S33 S34
S41 S42 S43 S44

➡ **Touchstone file: .S4P**

4Port Mixed-Mode S-parameters

			Stimulus			
			Differential		Common Mode	
			Port 1	Port 2	Port 1	Port 2
Response	Differential	Port 1	SDD11	SDD12	SDC11	SDC12
		Port 2	SDD21	SDD22	SDC21	SDC22
	Common Mode	Port 1	SCD11	SCD12	SCC11	SCC12
		Port 2	SCD21	SCD22	SCC21	SCC22

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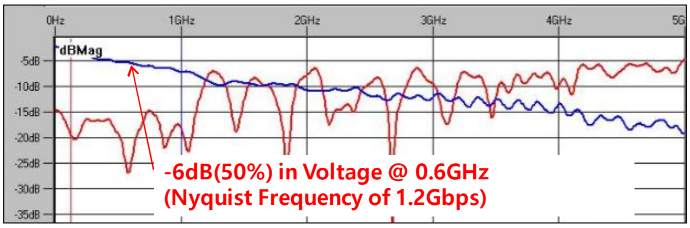
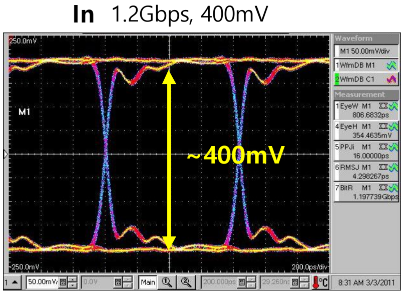
Measured Example of Lossy Transmission Line

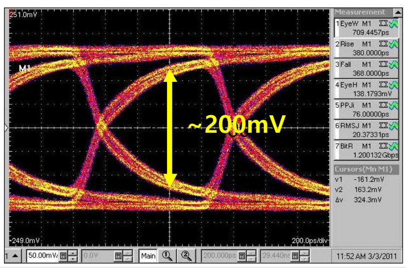
Frequency Domain: Insertion Loss, or S21 and EYE opening



In 1.2Gbps, 400mV



Out



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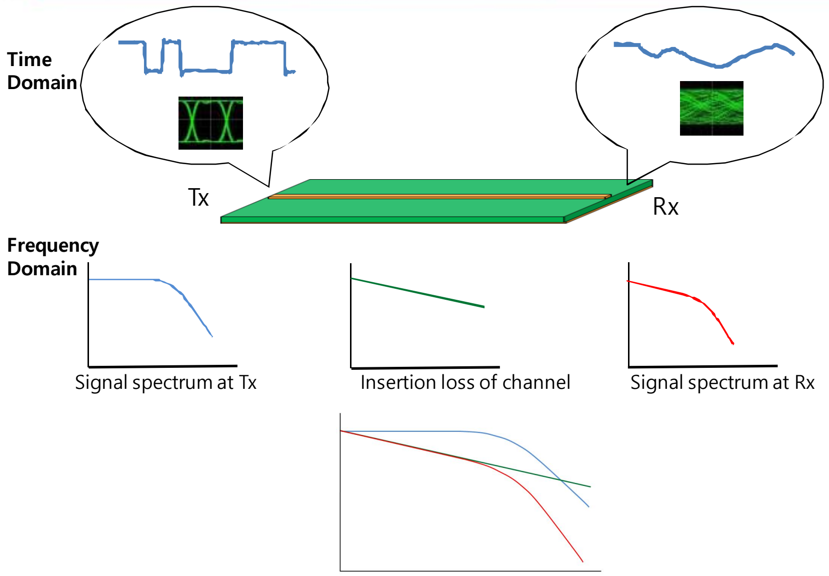
Signal attenuation in time and frequency domain



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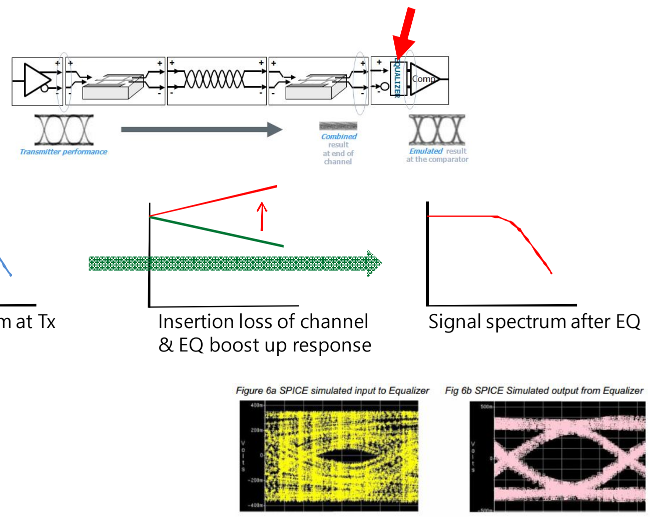
Compensation for loss

Equalization



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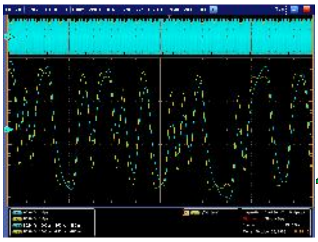
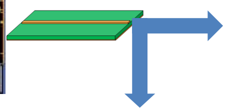
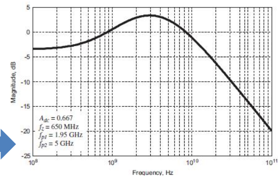
Equalization Example of USB3.0 standard

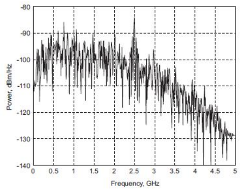


<waveform in time domain, 5Gbps
Blue: original, yellow: after EQ>

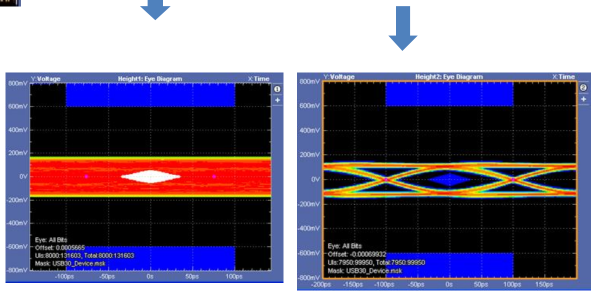




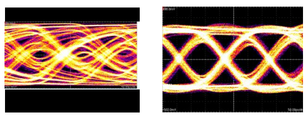
<CTLE Equalizer, high frequency boost up>



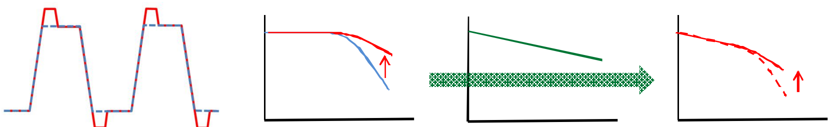
<Tx signal spectrum>



Compensation for loss

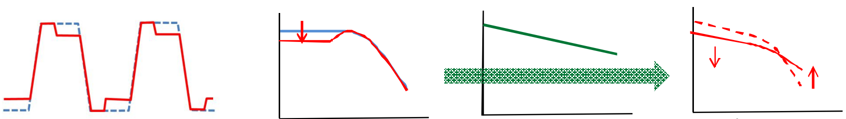


Pre-emphasis



Signal spectrum at Tx | Insertion loss of channel | Signal spectrum at Rx

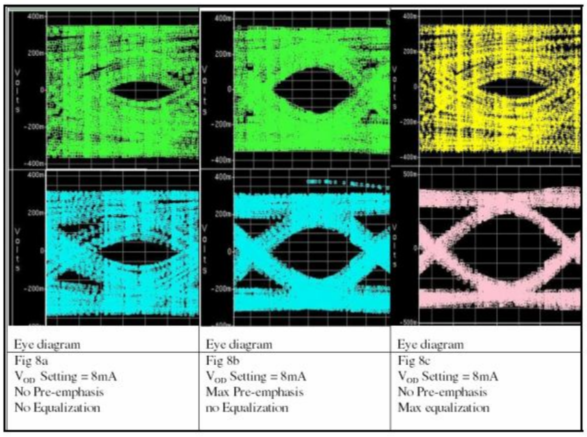
De-emphasis



Signal spectrum at Tx | Insertion loss of channel | Signal spectrum at Rx

Example of Loss compensation

Fig 8 40" Tyco backplane using a PRBS 10 pattern



<Source: Altera Corp.>

Pros and Cons of loss compensation

Equalization

✓EQ will amplify all high frequency component. Too much compensation can make more noise and jitter.

Pre-emphasis

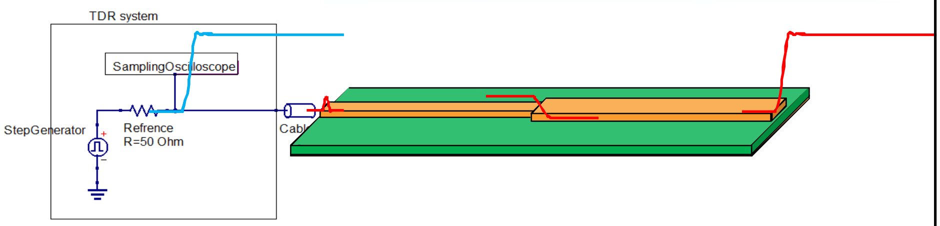
✓Pre-emphasis has higher power dissipation.
✓Faster edge speed, overshoot and undershoot can make more EMI issues.
✓Pre-emphasis can send more signal to the end of very lossy line.

De-emphasis

✓De-emphasis has less power dissipation.
✓Less near end crosstalk to adjacent channel

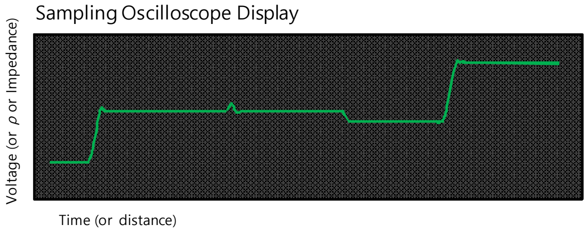
TDR (Time Domain Reflectometry)

How does TDR works?



$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_0}{Z_L + Z_0} \qquad Z_L = Z_0 \times \frac{(1 + \rho)}{(1 - \rho)}$$

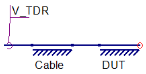
Sampling Oscilloscope Display

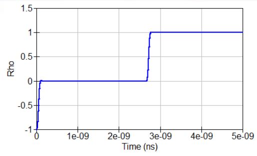


ρ = reflection coefficient, rho
Z_0 = reference Impedance
Z_L = DUT Impedance

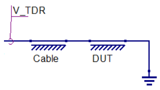
Typical TDR waveforms

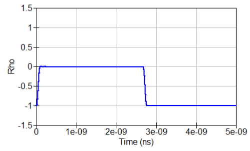
Open



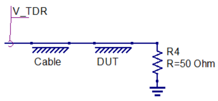


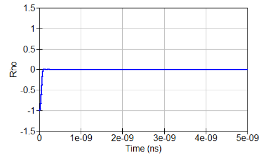
Short





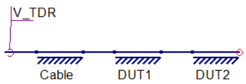
Load

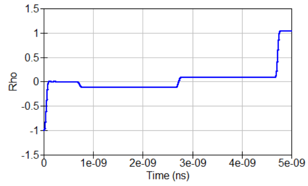




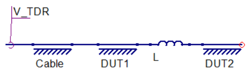
Typical TDR waveforms

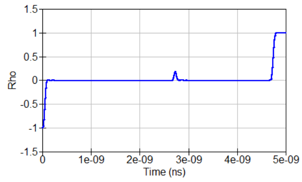
Impedance change



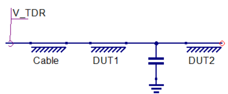


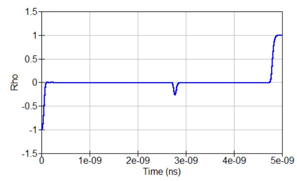
Inductive discontinuity





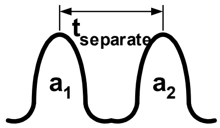
Capacitive discontinuity



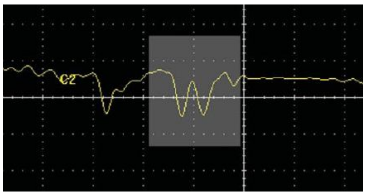


TDR Resolution

✓ Basic resolution, using t_{rise} **/ 2** rule:



To resolve a_1 and a_2 as separate discontinuities:
$t_{separate} > t_{TDR\_risetime}$ /2

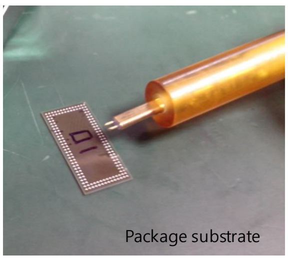


Rise time, ps	Resolution in air, mm	Resolution in FR4, buried run (v=0.446*C_{light}), mm
10	1.50	0.67
15	2.25	1.00
20	3.00	1.34
28	4.20	1.87
40	6.00	2.68
150	22.50	10.04

<source: Tektronix, Tested with 15ps, 80E10>

Rise Time and TDR Resolution Example(1)

Short trace, appx <10mm length

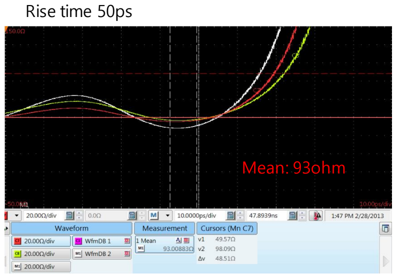


Resolution of TDR system

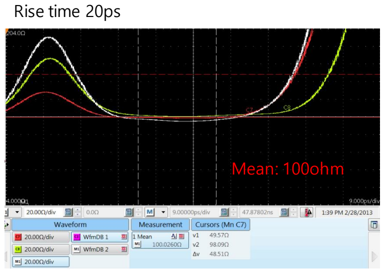
TDR System Risetime	Resolution	4X Resolution
10 ps	5 ps / 1 mm [0.04 in]	4 mm [0.16 in]
20 ps	10 ps / 2 mm [0.08 in]	8 mm [0.31 in]
30 ps	15 ps / 3 mm [0.12 in]	12 mm [0.47 in]
100 ps	50 ps/ 10 mm [0.39 in]	40 mm [1.57 in]
200 ps	100 ps / 20 mm [0.79 in]	80 mm [3.15 in]
500 ps	250 ps / 50 mm [1.97in]	200 mm [7.87 in]

<Source: IPC>

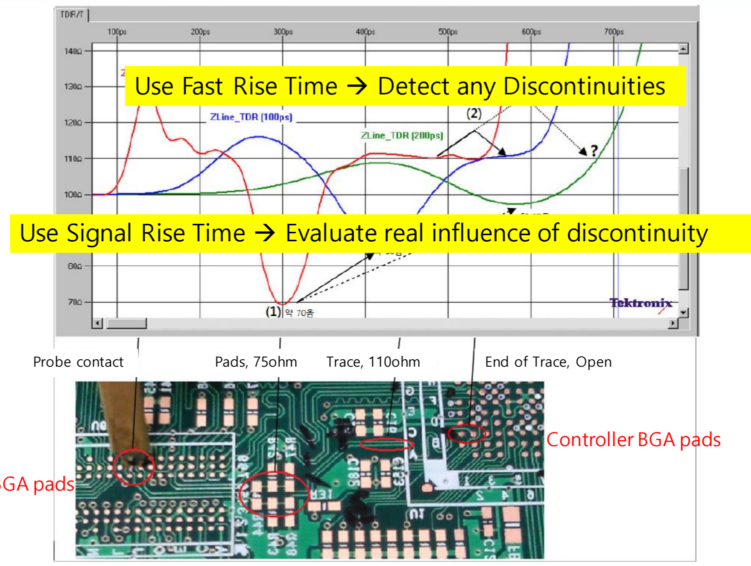
Rise time 50ps



Rise time 20ps



Rise Time and TDR Resolution Example(2)



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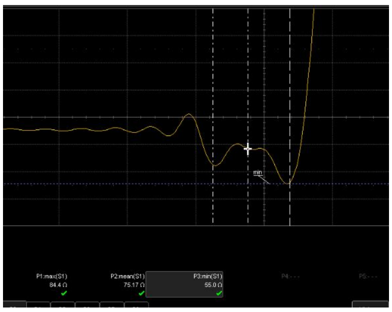
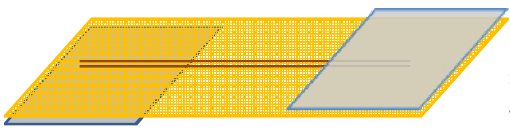
Measurement example

<Probing with Gigaprobes>





Metal Plane works as additional solid Reference(GND).
And they might make Impedance Lower.

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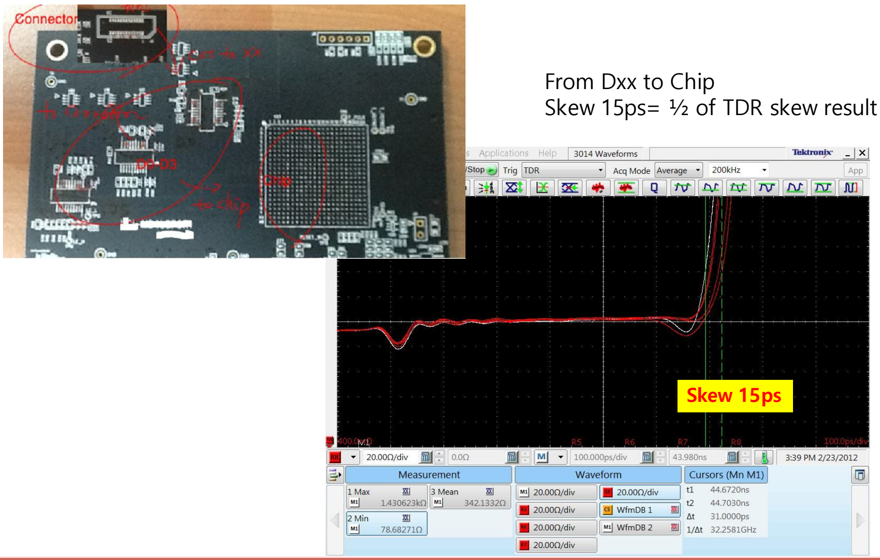
Time delay, Skew

From Dxx to Chip
Skew 15ps= ½ of TDR skew result



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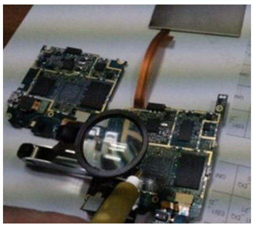
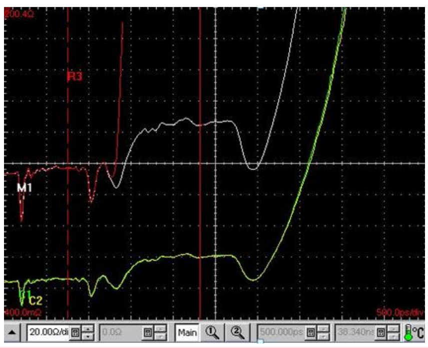
TDR Measurement Example: MIPI DSI traces



✓Impedance discontinuities
✓skew



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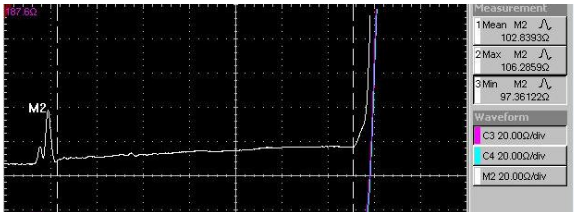
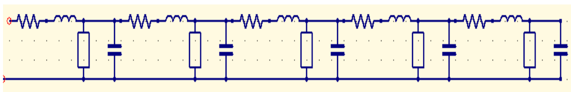
TDR waveform with Loss

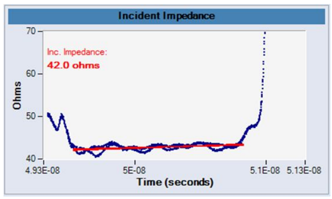


TDR waveform of Uniform Transmission Line with dribble up effect

Model of Lossy Transmission Line

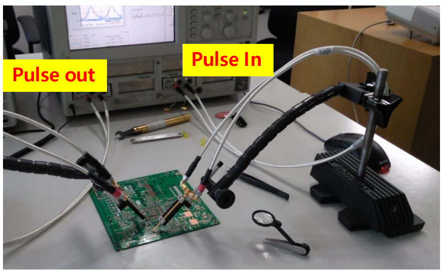


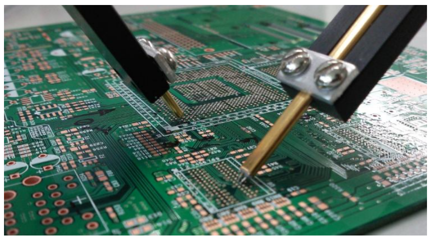
Incident Impedance



<Source: Introbotix>

TDT (Time Domain Transmission)

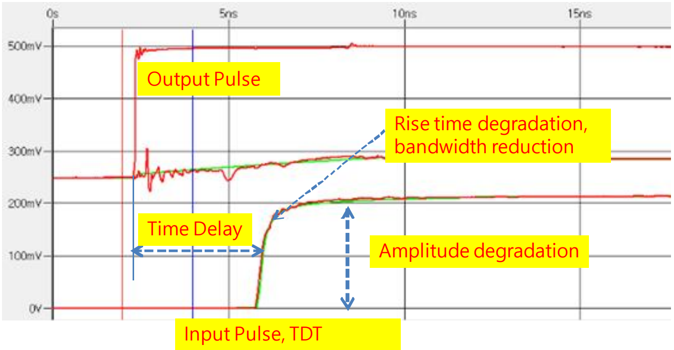




Measurement parameters

✓Time delay /Skew
✓Rise time degradation → Bandwidth
0.35/Tr
✓Waveform distortion by reflection

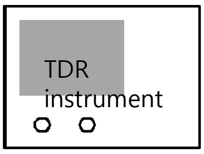
Example of TDT measurement

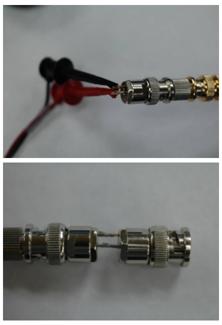


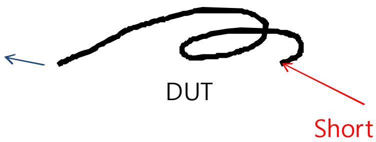
Output pulse should be acquired by low loss through connection.

$Tr_{DUT}=\sqrt{Tr_{Input}^2-Tr_{output}^2}$ BW(-3dB) of DUT= $0.35/Tr_{DUT}$

Connect to DUT (Probing Quality)

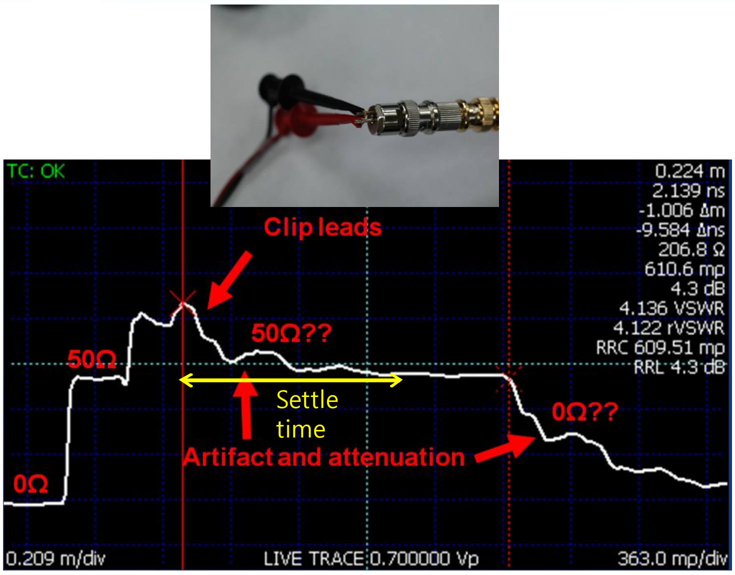






Coax cable, Zo=50Ohm
Length= 1m

Connect to DUT(Probing Quality)



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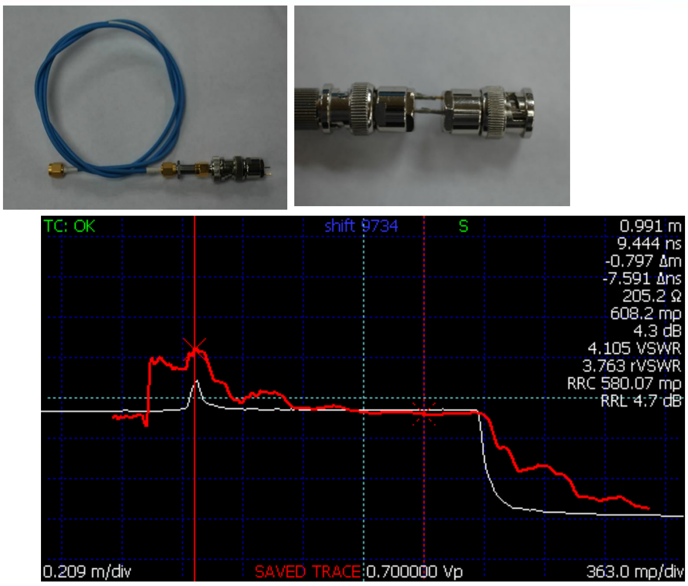
Connect to DUT (Probing Quality)



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TDR Probe Example(1)

✓ Hand Held Probe

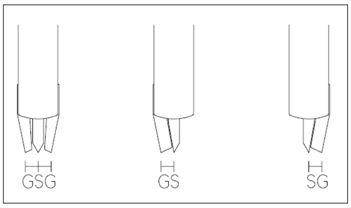
Tektronix, P8018

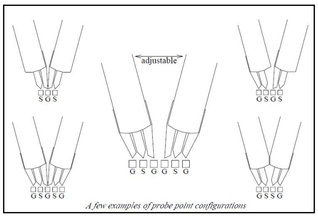
P80318

✓BW:~20GHz
✓Pitch: 0.5mm~4.2mm, adjustable
✓Signal to Signal for differential(odd mode)
✓Test Coupon and Large Pad

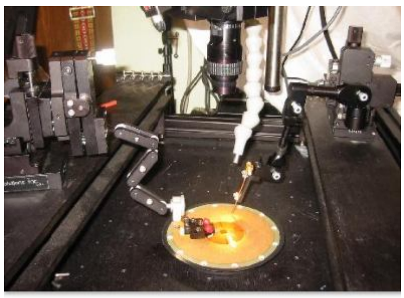
TDR Probe Example(2)

✓ RF Micro Probe





A few examples of probe point configurations



✓BW: ~ 40GHz, ~220GHz

✓Pitch: 50um ~1.25mm, fixed
✓Signal to Ground, G-S-S-G, etc.
✓Wafer, Die, Small pads

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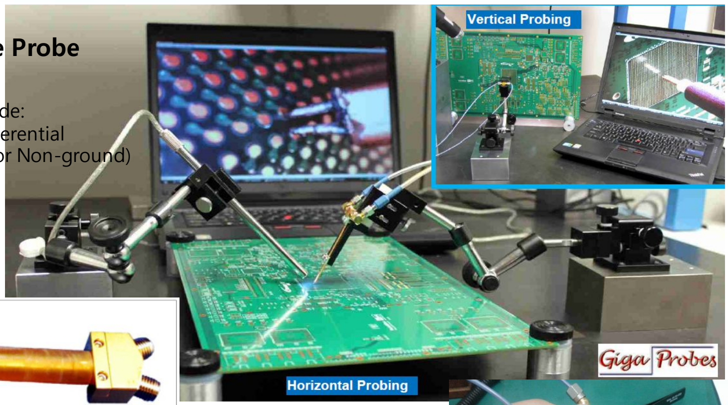
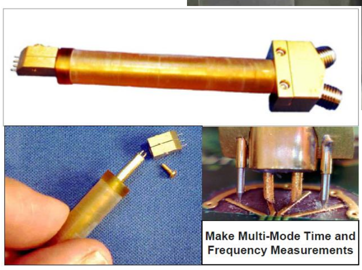
TDR Probe Example(3)

✓ **Multi Purpose Probe**

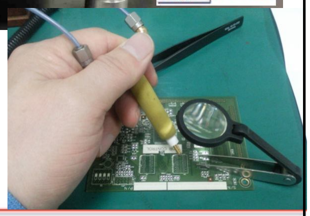
Convertible Multimode:
Single ⟷ Differential
(Ground or Non-ground)





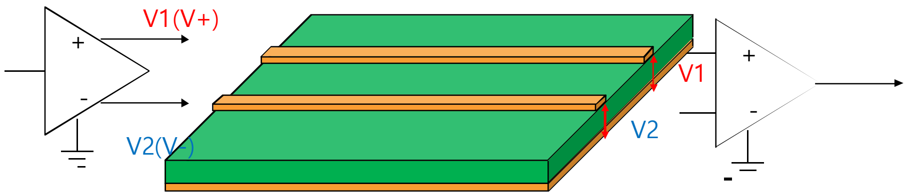
- ✓**BW: ~40GHz**
- ✓**Pitch: 200um~2mm**
- ✓**S-S, G-S-S-G, etc.**
- ✓**PCB pads**

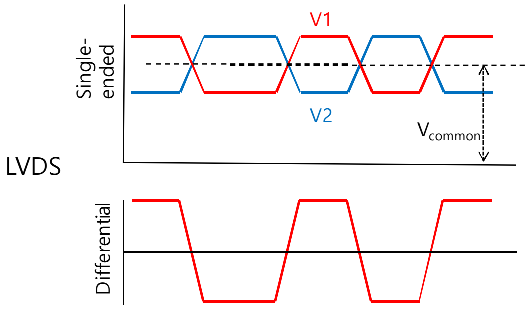
<Gigaprobes>



Differential Signal
Common mode signal
Differential Impedance
Common Impedance

Differential Signaling



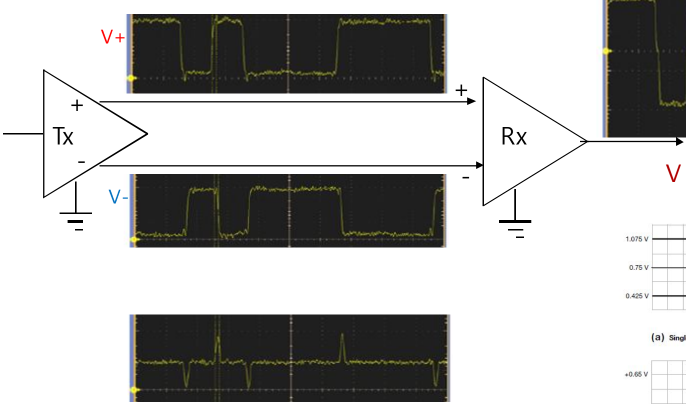


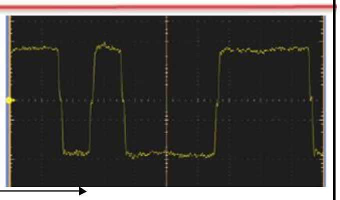
$V_{differential}$ = V1-V2

V_{common} = (V1+V2) /2

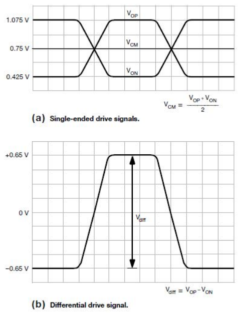
In AC coupled signal, V_{common} is 0

Mode conversion





V diff = (V+)-(V-)

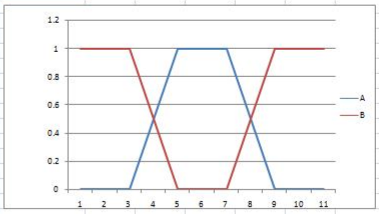


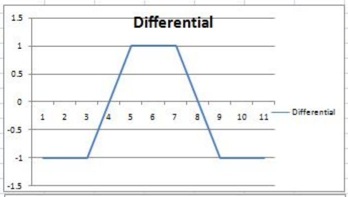
V_{cm} = (V+)+(V-) /2

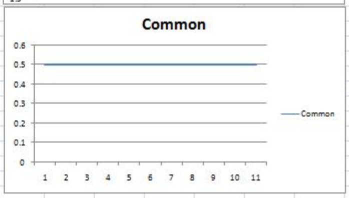
Differential to Common mode noise → EMI
Common to Differential Mode → Jitter, Noise

Mode Conversion

A	0	0	0	0.5	1	1	1	0.5	0	0	0
B	1	1	1	0.5	0	0	0	0.5	1	1	1
A-B(diff)	-1	-1	-1	0	1	1	1	0	-1	-1	-1
(A+B)/2(comm)	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5

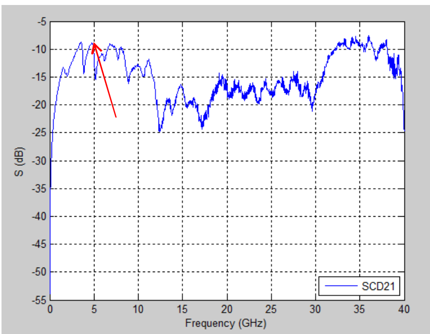


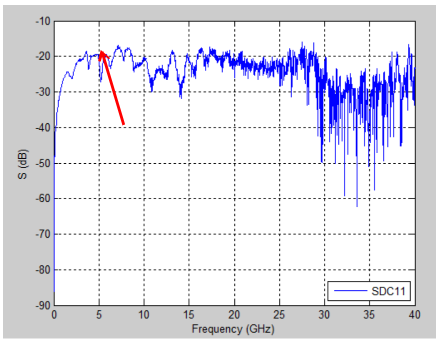




1. Edge mismatch
2. abberation one line
3. skew
4. amplitude mismatch

Mode Conversion in Frequency Domain





Differential to Common mode noise
→ EMI

@10Gbps, Nyquist 5GHz, -10dB (30%)
1Vdiff → 0.3Vcomm

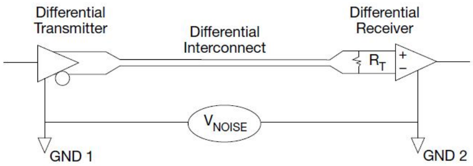
Common to Differential Mode
→ Jitter, Noise

@5GHz, -20dB (10%)
0.3Vcomm → 0.03Vdiff

Advantage of Differential Signaling

Advantages

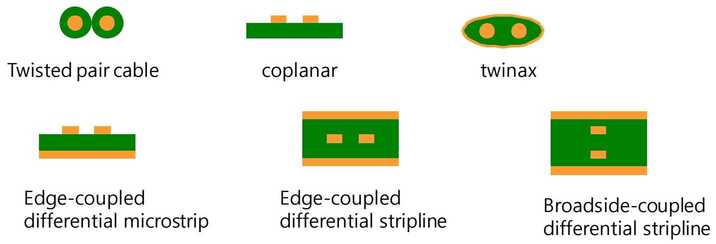
- ✓ Common mode Noise rejection
- ✓ Less dI/dt → Less Ground Bounce, Less Rail collapse Noise, less EMI
- ✓ Higher Gain at the receiver
- ✓ Tightly coupled differential line
  → Robust to Cross talk, discontinuity in the return path, less EMI



Disadvantages

- ✓ EMI from not properly balanced pair
- ✓ Twice Number of signal lines, Layout complexity
- ✓ New principles and design guidelines to understand

Differential Pair

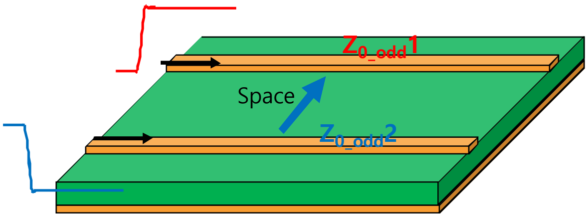


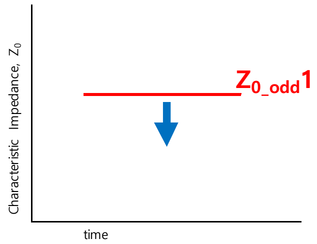
✓ Good differential pairs have;

1. Constant impedance for the differential signal.
2. Same length/Time delay match between two lines.
3. Exactly same both transmission lines – symmetry
4. The greater the coupling the more robust the differential signal
   - noise immunity benefit, discontinuity and imperfection

Differential Impedance – Odd mode

✓**Odd-mode Impedance is decrease as coupled line is closer.**





Each pulses has opposite rise/fall directions(polarities)

This is called as Odd-mode, **$Z_{0\_odd}1$ = Odd-mode Impedance**

2 x $Z_{0\_odd}1$ = Differential Impedance, Z_{diff}

$Z_{0\_odd}2$ has the same behavior with $Z_{0\_odd}1$

$$Z_{differential} = Z_{0\_odd} + Z_{0\_odd}$$

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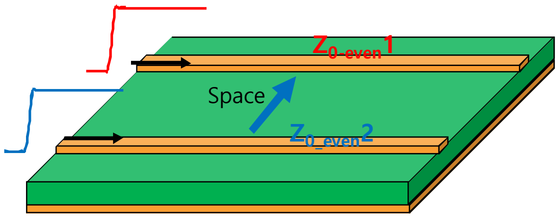
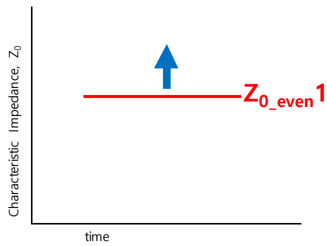
Common Impedance – Even mode

✓**Even-mode Impedance is increase as coupled line is closer.**





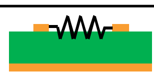
Each pulses has the same rise/fall directions(polarities)

This is called as Even-mode, **$Z_{0\_even}1$ = Even mode Impedance**

1/2 x $Z_{0\_even}1$ = Common Impedance, Z_{comm}

$Z_{0\_even}2$ has the same behavior with $Z_{0\_even}1$

$$Z_{comm} = \frac{1}{2}(Z_{0\_even} + Z_{0\_even})$$



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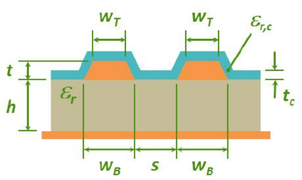
Impedance Calculator

Diff. Coated Microstrip Line



Line Parameters

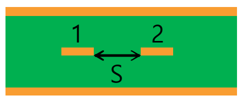
Parameter	Value	Unit
wT	250	um
wB	260	um
s	250	um
h	200	um
t	35	um
tC	13	um
Er	4.3	
Er,c	3.3	

Calculations

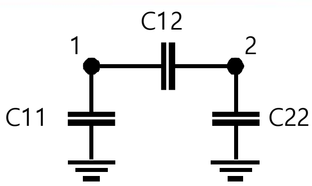
Parameter	Value	Unit
Z0	99.6	Ohm
Zodd	49.8	Ohm
Zeven	65.3	Ohm
ErEff	2.9	
Cs	114	pF/m
Ls	282.7	nH/m
Velocity	176164496	m/s
PropDelay	5.677	ns/m

<Calculated by STLC (Sequid Transmission-Line Online-Calculator)>

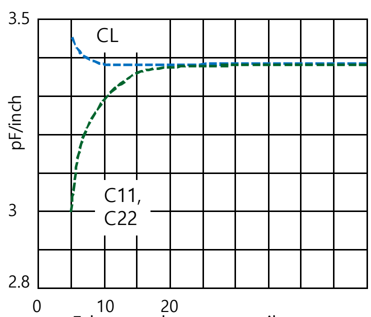
Capacitive coupling between two lines

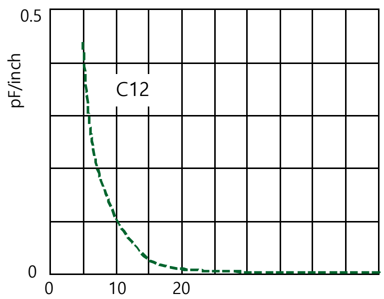


Stripline cross section



Equivalent capacitance circuit model





CL=C11 + C12

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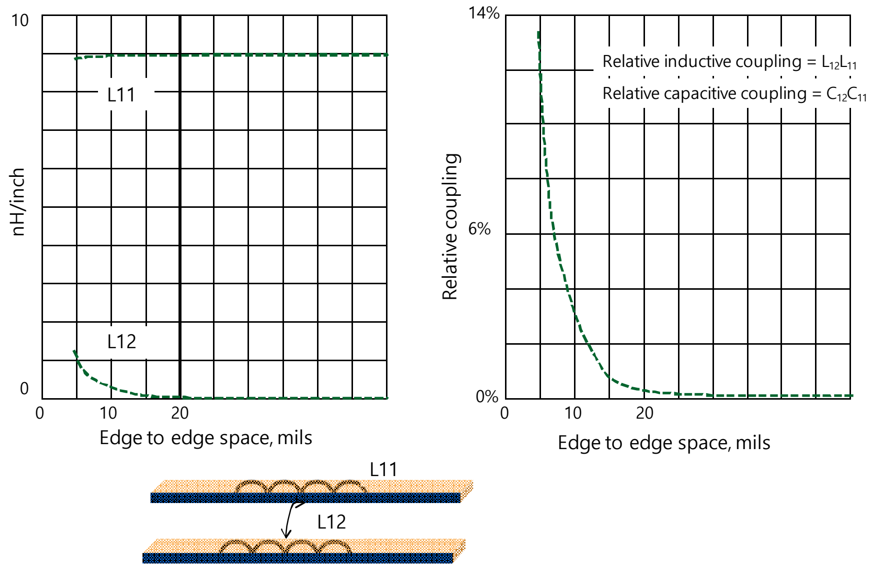
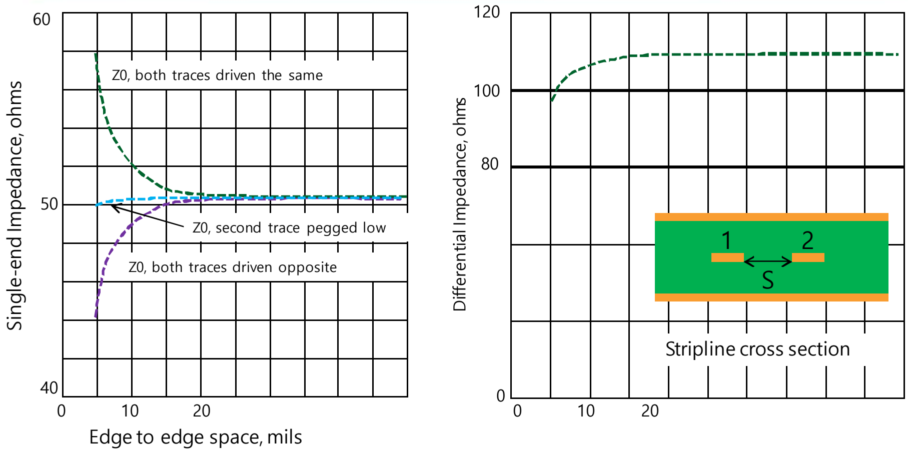
Inductance coupling between two lines

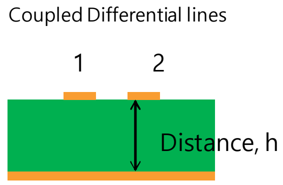


Differential Impedance with Coupling

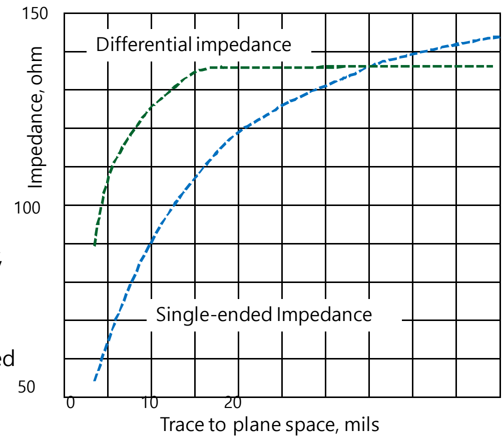


✓ Tightly coupled differential line
→robust to Cross talk, discontinuity in the return path, less EMI

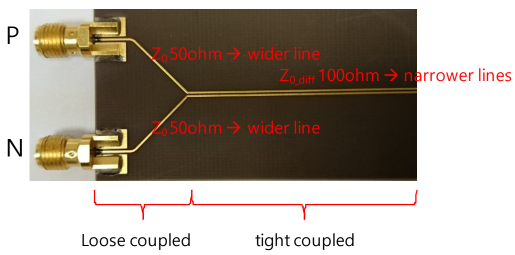
Differential Impedance with Reference plan



If the reference plane moves far away, return current of each traces will overlap and cancel each other as polarities are opposite.
Return current of trace 1 will be carried by trace 2.



Tight or loose coupling for differential lines?



✓Tight coupled differential lines have advantages on;

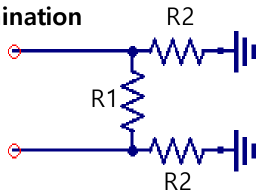
➡ Robust to crosstalk, Board space

✓Loose coupled differential lines have advantages on;

➡ Loss

Termination for Z_{diff} and Z_{comm}

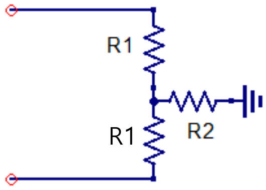
pi termination



$$R1 = \frac{2\,Z_{even}Z_{odd}}{Z_{even} - Z_{odd}}$$

$$R2 = Z_{even}$$

tee termination



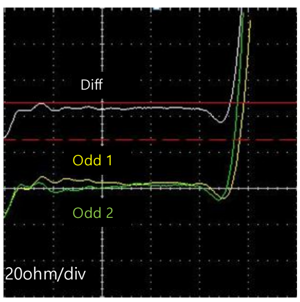
$$R1 = Z_{odd}$$

$$R2 = \frac{1}{2}(Z_{even} - Z_{odd})$$

✓ **Is terminating the common signal going to eliminate the common signal?**

Example of TDR Analysis on Diff Traces

- ✓ Impedance unbalance
- ✓ Skew
- ✓ Differential signal Distortion
- ✓ Common mode noise



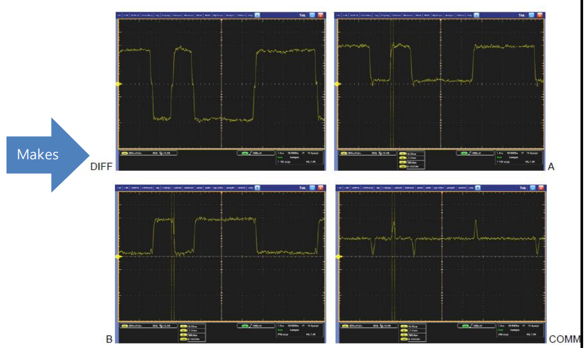


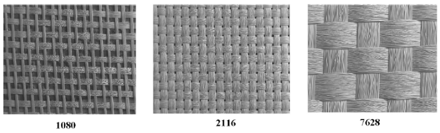
Figure 8. Differential signal example with excess time delay between the positive and negative inputs.

Glass Weave induced Skew

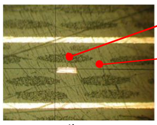
Glass weave effect of FR4 on differential impedance

Unbalance and Skew in differential pairs

Pitch~17x21mil   Pitch~23x31mil



<Typical laminate weaves>



<5mil trace>

<source: Teraspeed, Teradyne>

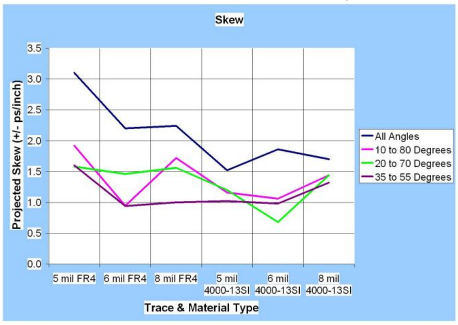


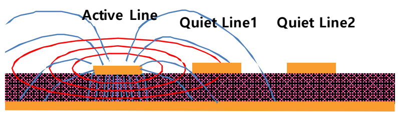
Figure 11: Projected Skew vs. Trace Routing Angle, Trace Width & Material Type

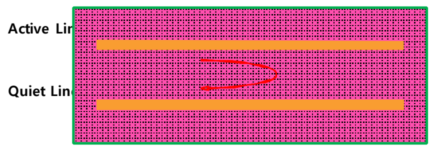
How to reduce the risk of weave induced skew

- ✓Wider traces
- ✓Zig-zag routing (45˚)
- ✓Use lower Dk glass
- ✓Match diff pitch to weave pitch: eg. 8/8/8mil for 17mil weave

Crosstalk

Cause of Crosstalk





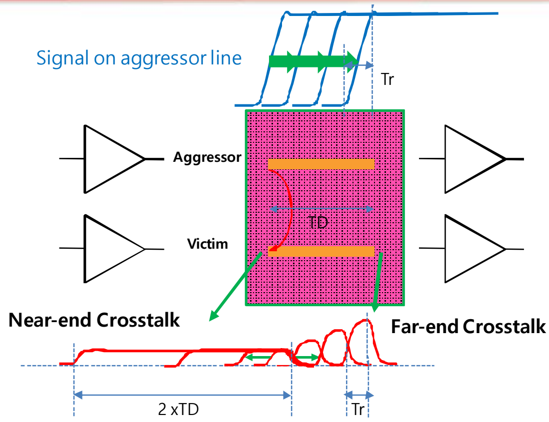
Electric Field Lines
Magnetic Field Lines in Microstrip

Capacitive coupling from Electric field → Mutual Capacitance (Cm)

Inductive coupling from Magnetic field → Mutual Inductance (Lm)

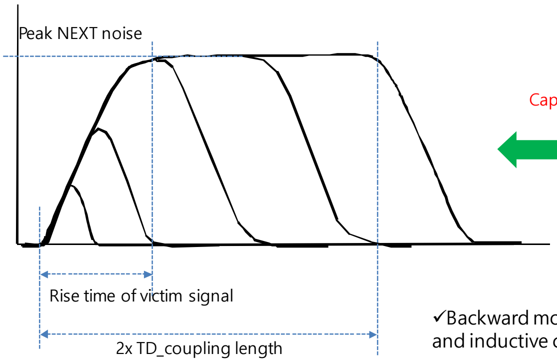
$$I_{noise,\ Cm} = C_m \text{ x } \frac{dV_{driver}}{dt} \qquad V_{noise,\ Lm} = L_m \text{ x } \frac{dI_{driver}}{dt}$$

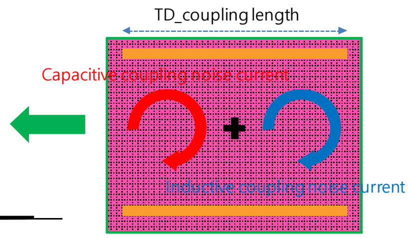
Near and Far end Crosstalk



Crosstalk induced noise on victim line can affect on the signal integrity at near-end and far-end.

Near-end Crosstalk (NEXT)





✓Backward moving NEXT noise is sum of Capacitive and inductive coupling noise.

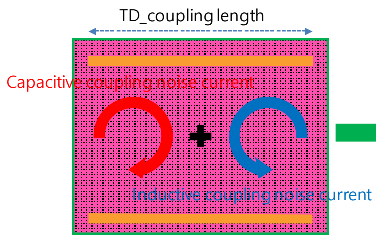
✓With same polarity with aggressor Signal

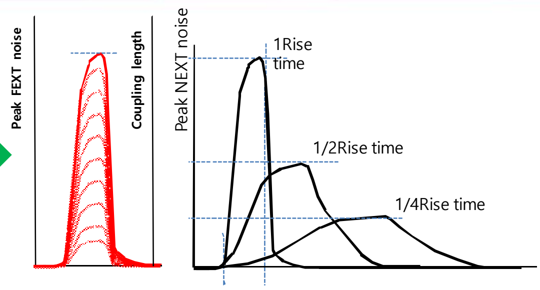
✓Peak NEXT noise is independent with the rise time when 2*TD is longer than the rise time.

$$NEXT = \frac{Vb}{Va} = k_b$$

Va= Voltage of aggressor
Vb= Voltage noise in the backward
k_b= Backward coefficient

Far-end Crosstalk (FEXT)





✓As inductive coupling current has opposite direction with signal current, forward moving FEXT noise is difference between Capacitive and inductive coupling noise.

✓If capacitive coupling is larger than inductive coupling, the polarity is same with aggressor Signal.

✓If inductive coupling is larger than capacitive coupling, the polarity is opposite to aggressor signal.

✓The Peak FEXT noise scales with the coupling length.

✓dV/dt and dI/dt generate coupling noise

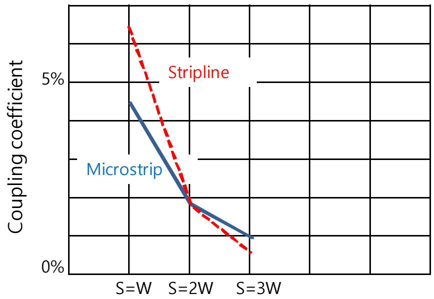
✓As the rise time increases, the width of noise increases and the peak of noise decreases.

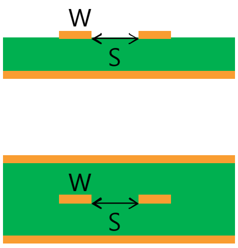
$$FEXT = \frac{Vf}{Va} = \frac{TD}{Tr} \times v \times k_f$$

Va= Voltage of aggressor
Vf= Voltage noise in the forward
v= velocity of the signal
k_f= FE coupling coefficient

Coupling

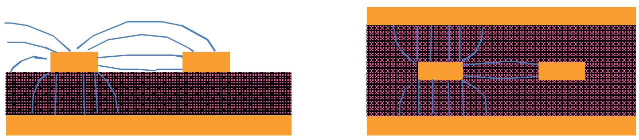
Example of coupling coefficient





Coupling decreases exponentially with the distance of two lines.
Space >= 3 x Width, it's <<1%.

Crosstalk trend in Microstrip and Stripline

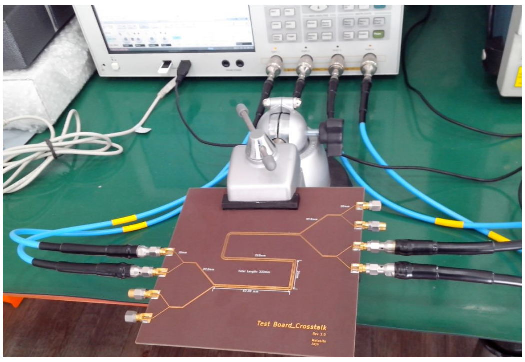


✓Stripline builds stronger coupling with reference planes than microstrip
✓It exhibits less coupling to adjacent lines → less crosstalk

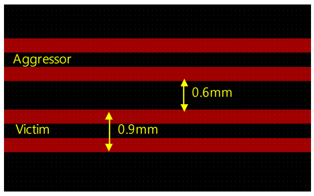
✓For stripline, mutual capacitance and mutual inductance are more balanced.
✓It makes less far-end crosstalk noise.
✓Thick solder mask on microstrip or embedded microstrip can reduce crosstalk.

✓Strong coupling with reference plans makes more capacitance and lower impedance.
✓Lower impedance exhibit less coupling to adjacent lines.

Xtalk measurement



<The setup for Far-end Crosstalk measurement, differential>

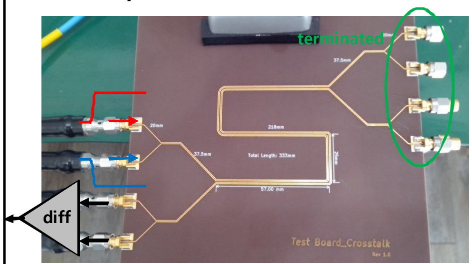


Two tightly coupled differential lines, 0.3x0.3x0.3mm
Space between differential lines: 0.6mm

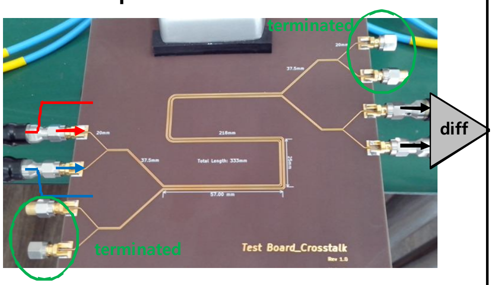
Coupled lines length: 220mm (8.67inch)
Total length: 333mm (13.1inch)

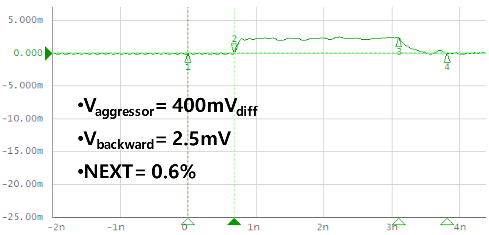
Crosstalk Measurement

Setup for NEXT measurement

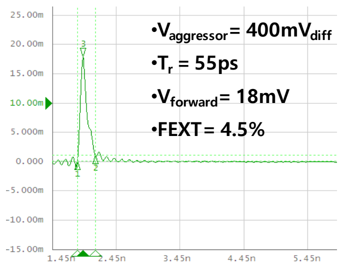


Setup for FEXT measurement





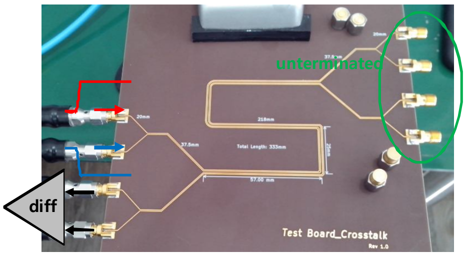
- $V_{aggressor}$ = 400mV$_{diff}$
- $V_{backward}$ = 2.5mV
- NEXT = 0.6%



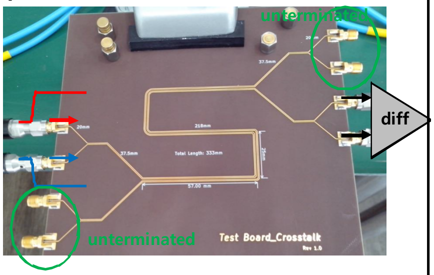
- $V_{aggressor}$ = 400mV$_{diff}$
- T_r = 55ps
- $V_{forward}$ = 18mV
- FEXT = 4.5%

Crosstalk Measurement

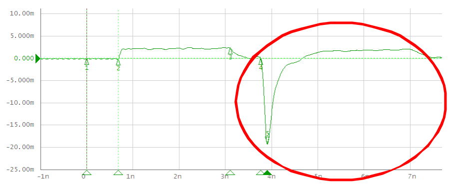
Setup for NEXT measurement- un-terminated

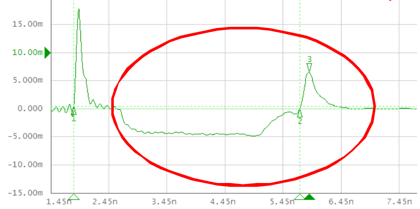


Setup for FEXT measurement- un-terminated

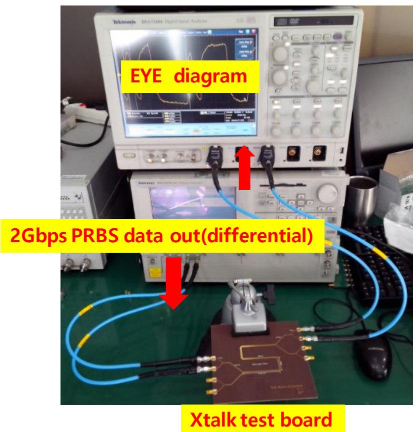


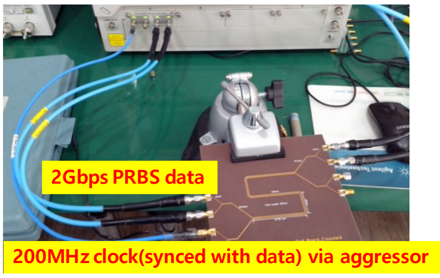
Additional noise from the multi reflection from un-terminated ports

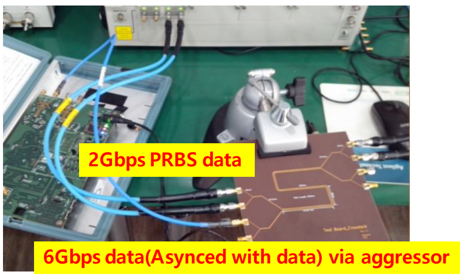




FEXT affect on EYE diagram

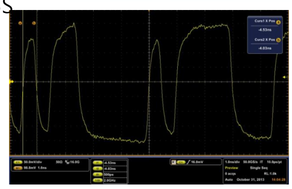




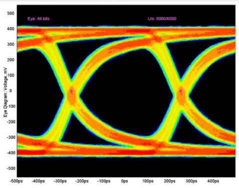


Example of Xtalk on EYE diagram

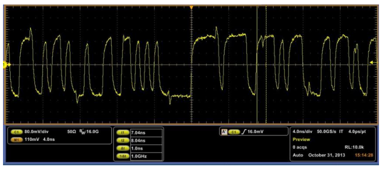
2Gbps PRBS



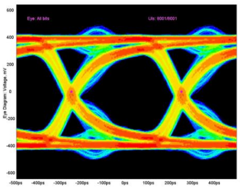
TJ= 106ps



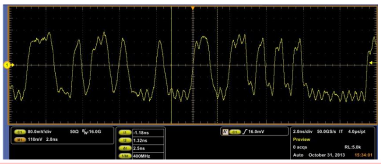
w. 200MHz Sync clock on aggressor



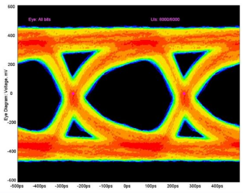
TJ= 146ps



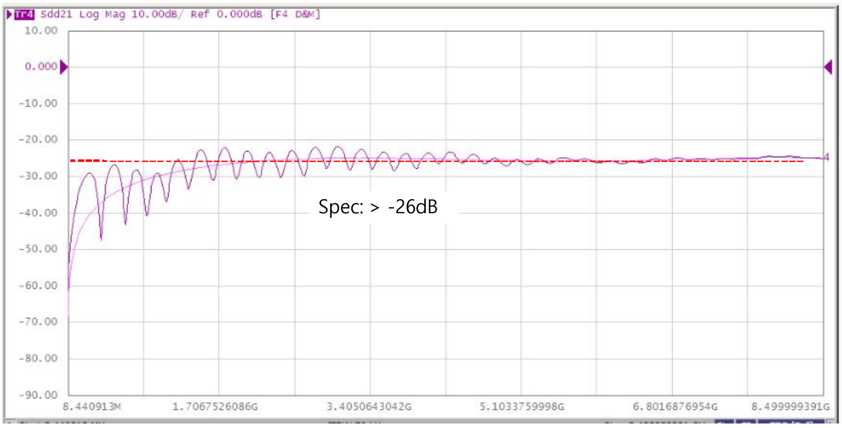
w. 6Gbps Async data on aggressor



TJ= 184ps



Example of Crosstalk in Frequency domain

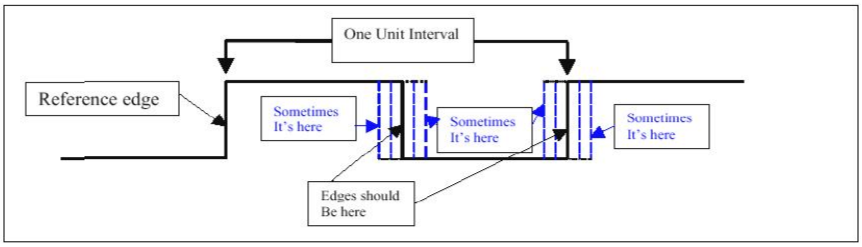


- ✓Far-end Noise(Xtalk) with and without termination, test board
- ✓Far-end noise(Xtalk) spec of Displayport standard(1.1)

Fundamental of EYE diagram and Jitter

What is the Jitter ?

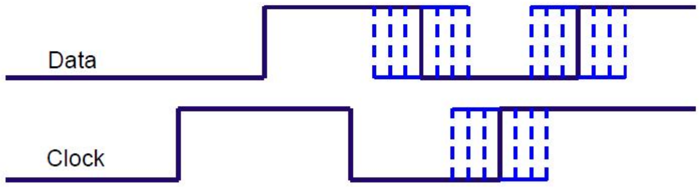
- What is jitter?
  - "The deviation of an edge from where it should be"
  - *ITU Definition of Jitter: "Short-term variations of the significant instants of a digital signal from their ideal positions in time"*



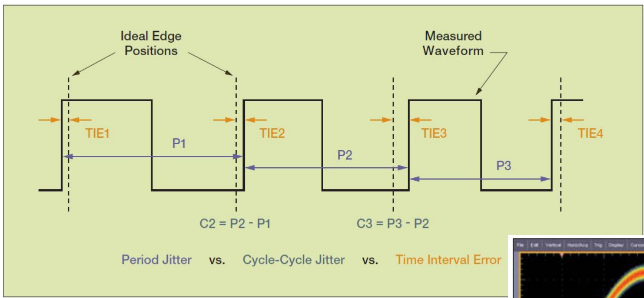
Jitter is a major signal integrity problem at high speed data rates

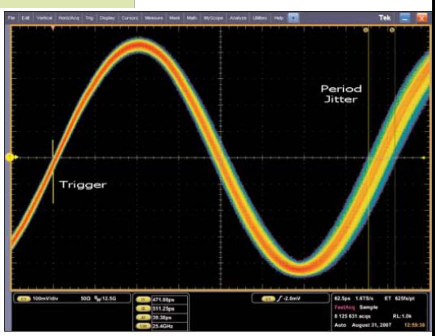
Why Do We Care about Jitter

- Simply put, too much jitter causes errors.



Jitter Concept and Terms





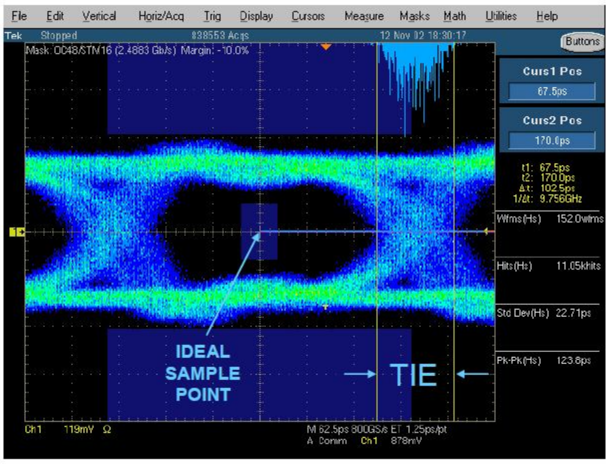
✓Period Jitter (PJ)

✓Cycle to Cycle Jitter(CCJ)

✓Time Interval Error(TIE)

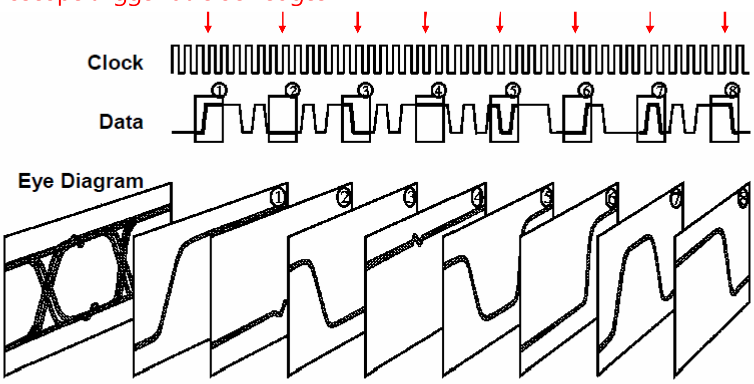
Time Interval Error (TIE)

✓Jitter showed in EYE diagram is TIE



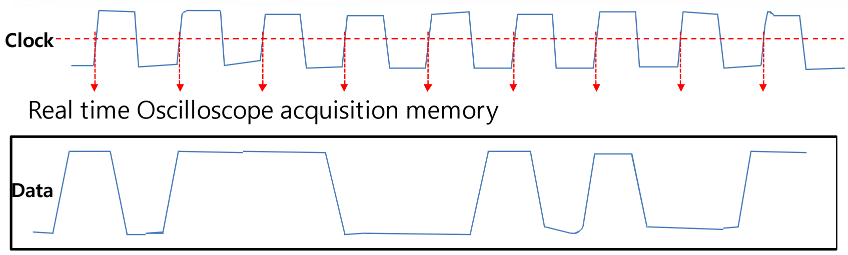
Construction of EYE diagram_method 1

Oscilloscope trigger at clock edges



✓Draw EYE with each 1 UI(bit) waveforms of realtime oscilloscope's each acquisition
✓Two channel for clock and data acquisition
✓EYE with Long term monitoring or desired amount of UIs

Construction of EYE Diagram_ method 2



✓Draw EYE with waveforms of each Bit from consecutive data stream.
✓Realtime acquisition with long memory required
✓Parameter's consecutive change over time (time trend) can be observed
✓Relatively short time acquisition than other method
✓Post processing software required

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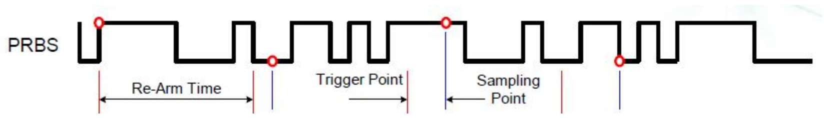
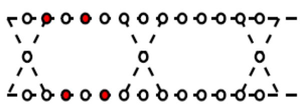
Construction of EYE diagram_method 1





✓Draw EYE with sample points of each trigger event
✓Sampling oscilloscope (or ET mode in Realtime Scope) method
✓EYE over long time change
✓Higher bandwidth, lower Jitter and noise floor on Sampling oscilloscope

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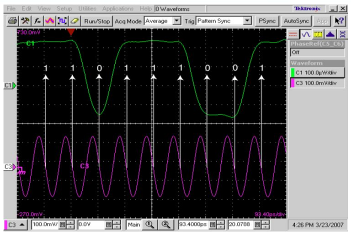
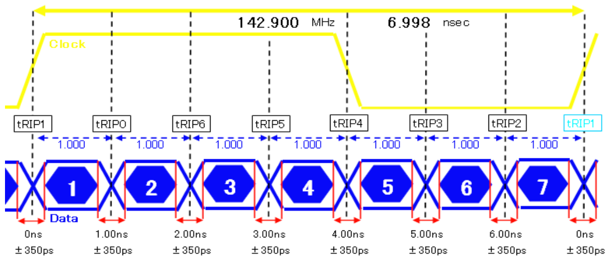
Reference Timing (Ideal Edge Position) for EYE/Jitter

- ✓ Clock signal

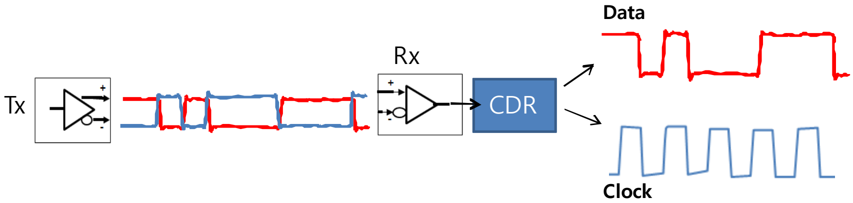


- ✓ Explicit Edge
  (e.g. LVDS, TMDS)

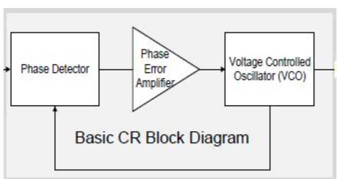


- ✓ Suppose Constant Clock
- ✓ Clock recovery (Embedded clock on serial data)

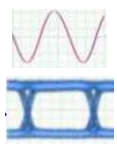
Clock Recovery _ Embedded clock



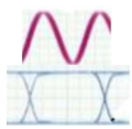
Clock Recovery and PLL Loop BW



When PLL Loop BW is narrow
→recovered clock has low jitter
→ Measured data jitter is high

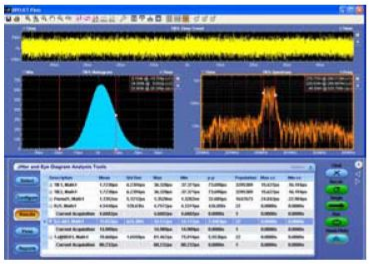


When PLL Loop BW is wide
→recovered clock has high jitter
→Measured data jitter is low



Many Jitter Terms

- Random Jitter (RJ)
- Deterministic Jitter (DJ)
  - Periodic Jitter (PJ)
  - Sinusoidal Jitter (SJ)
  - Duty Cycle Distortion (DCD)
  - Data-Dependent Jitter (DDJ)
  - Inter-Symbol Interference (ISI)
- Total Jitter ~ (TJ or TJ@BER)
- Bit Error Rate (BER)
- Eye Width @BER
  - versus Actual or Observed Eye Width



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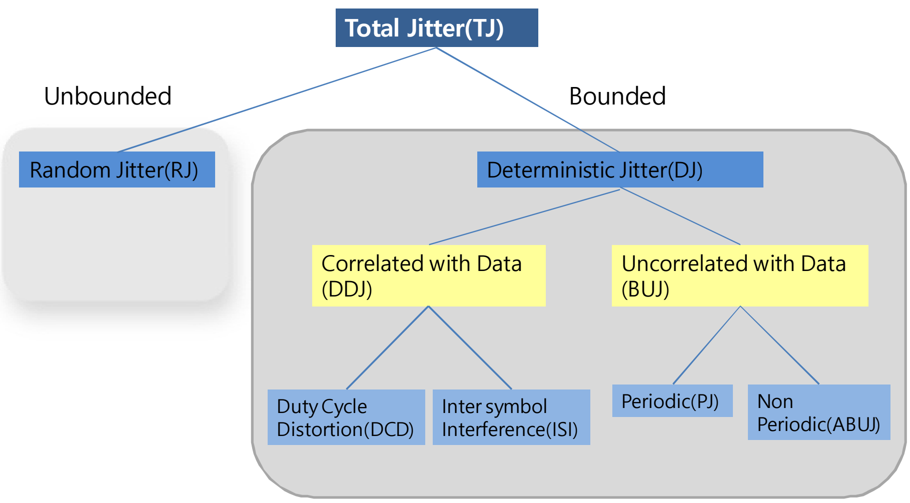
Jitter Decomposition



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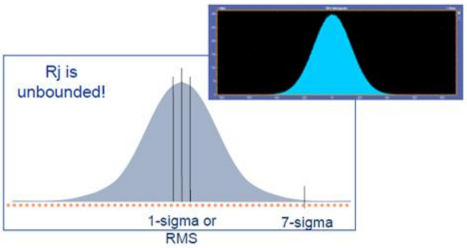
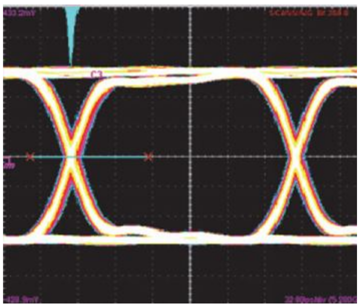
Random Jitter

✓Uncorrelated with data pattern
✓Unbounded, Increase with bit amount
✓ Measured in RMS

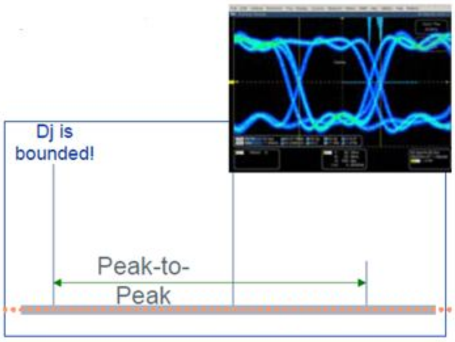




✓Common source:
Thermal noise, PLL of Tx, Noise of retiming in Tx

Deterministic Jitter (DJ)

✓Repeatable, Predictable
✓Bounded
✓Correlated with data or Uncorrelated with data

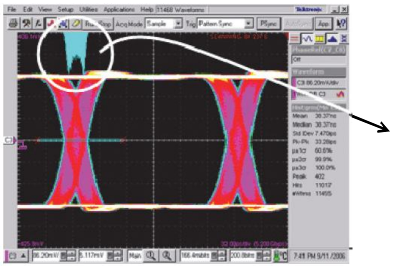


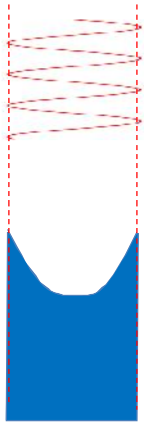
✓**DJ component**

- PJ / SJ : Periodic Jitter
- DDJ / ISI : Data Dependant Jitter / Inter Symbol Interference
- DCD: Duty Cycle Distortion
- ABUJ: Asynced Boundary Uncorrelated Jitter

Deterministic Jitter
- PJ/SJ (Periodic Jitter/Sinusoidal Jitter)

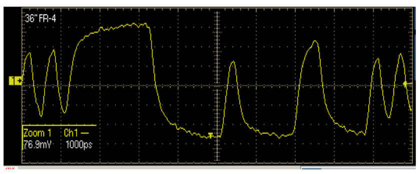
- ✓ Uncorrelated, Bounded
- ✓ PJ includes any jitter at a fixed frequency/period.
- ✓ Easy to measure
- ✓ Source: Power supply noise, Crosstalk, EMI
- ✓ SJ is PJ at just one frequency

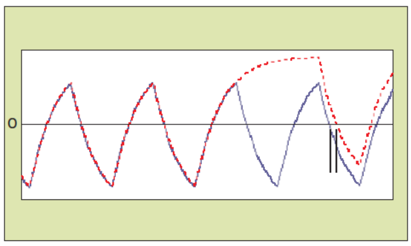




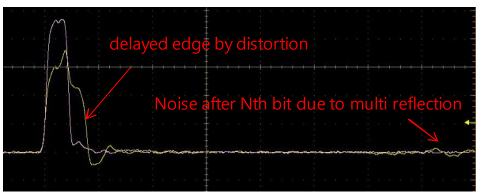
Deterministic Jitter
- DDJ/ISI (Data Dependant Jitter/Inter Symbol Interference)

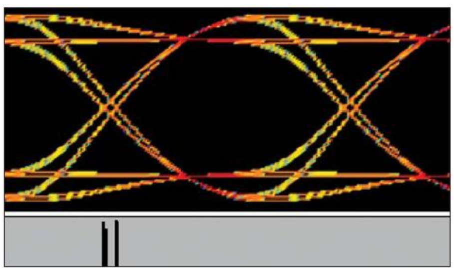
- ✓Correlated with data pattern
- ✓Bounded
- ✓ Source: Bandwidth limitation / Loss





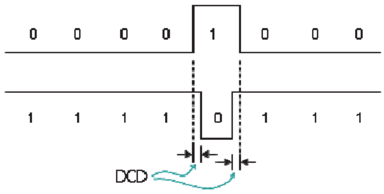
- ✓ Source: Reflections



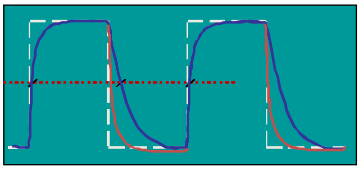


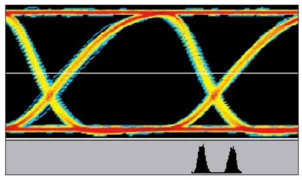
Deterministic Jitter
- DCD (Duty Cycle Distortion)

✓ Different Positive/Negative Duty Cycle

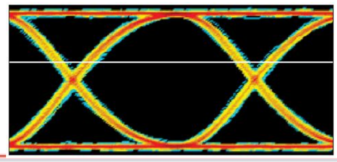


✓ Non-symmetrical Rise/Fall Time



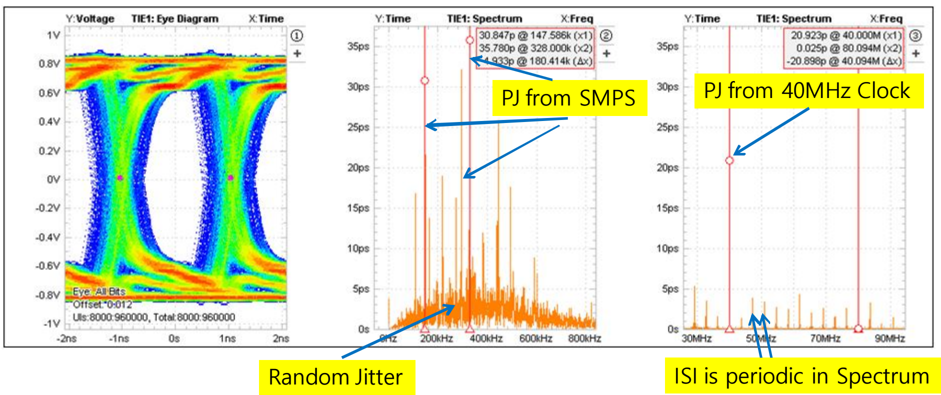


✓ Incorrect Detection Threshold

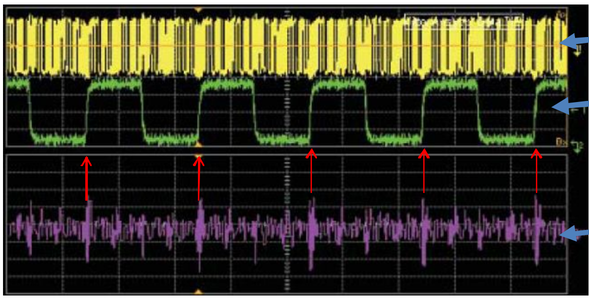


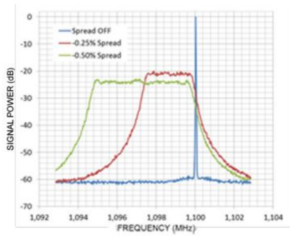
Jitter Spectrum

✓Each Jitter components can be distinguished in Frequency domain.

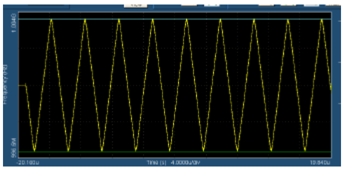


Time Trend





SSC measurement



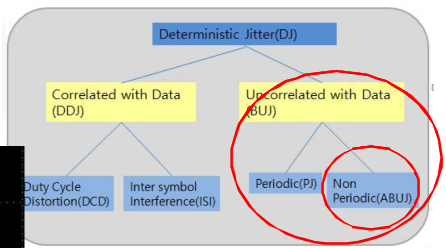
Aperiodic Boundary Uncorrected Jitter(ABUJ)

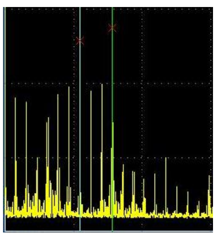
✓Jitter that is deterministic and uncorrelated with data can be periodic or aperiodic.

✓Periodic is easy to measure but, Aperiodic is not.

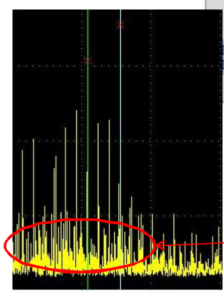
✓ABUJ is often caused by Xtalk

Bounded





<Jitter Spectrum w/o Xtalk>



ABUJ caused by Xtalk make RJ look bigger

<Jitter Spectrum w Xtalk>

Summary of Jitter acronym

	acronym	bounded/ unbounded	correlated/ uncorrelated	periodic/ aperiodic	Example cause
Random Jitter	RJ	Unbounded	Uncorrelated	Aperiodic	Thermal noise
Deterministic Jitter	DJ	Bounded	Either	Either	Inter-Symbol Interference
Periodic Jitter	PJ	Bounded	Either	Periodic	Power supply feed-through
Sinusoidal Jitter	SJ	Bounded	Uncorrelated	Periodic	Electromagnetic interference
Data-Dependent Jitter	DDJ	Bounded	Correlated	Aperiodic	Impedance mismatch
Duty-Cycle Distortion	DCD	Bounded	Correlated	Periodic	Clock asymmetry
Inter-Symbol Interference	ISI	Bounded	Correlated	Aperiodic	Non-uniform frequency response of a transmission line
Bounded Uncorrelated Jitter	BUJ	Bounded	Uncorrelated	Aperiodic	Crosstalk

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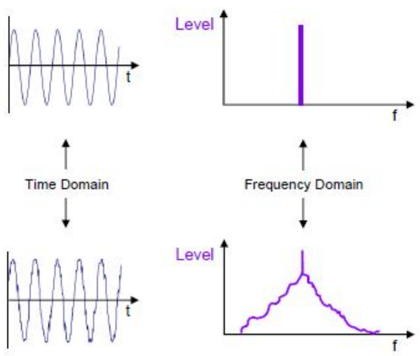
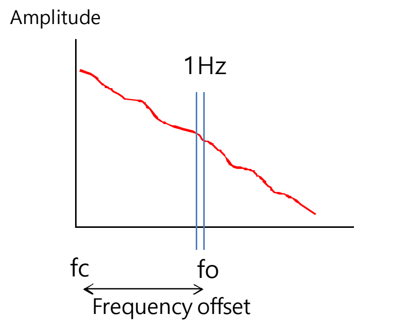
Phase Noise

- ✓Phase noise is fluctuation on the phase of the signal
- ✓Phase noise is correlated with Jitter in time domain
- ✓Clock signal only (50% duty cycle)
- ✓Highest sensitivity (fS)

✓Sideband power of 1Hz Bandwidth at fo





Phase Noise L(f) : dBc/Hz @ offset

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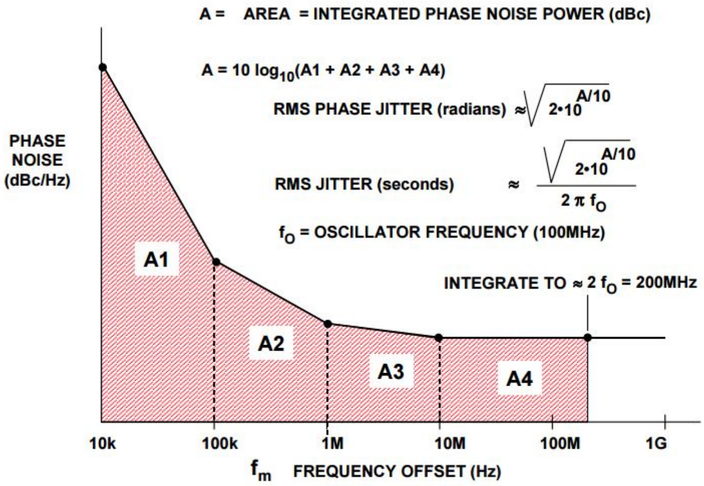
Jitter from Phase Noise



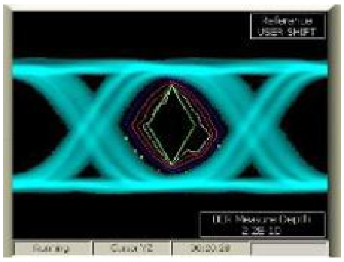
<Calculation Jitter from Phase Noise, source Analog Device>

Phase Noise Measurement Example

<source: Rohde&Schwarz>

Total Jitter @ BER

- **Total Jitter**
  - Estimated jitter for a large population: e.g. 10^{12} bits
- **BER: Bit Error Rate/Ratio**
  - Method to describe expected or measured data stream error rate or ratio of good bits to bad bits.
  - Example: In 10^{12} Bits, only one error is allowed => BER = 10^{-12}



Measured EYE diagram and estimated EYE open @BER

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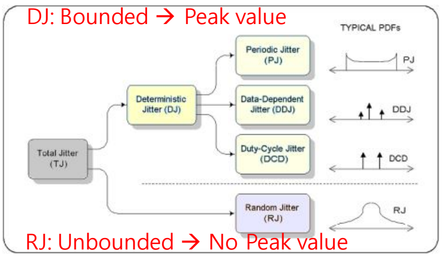
Total Jitter & Bathtub

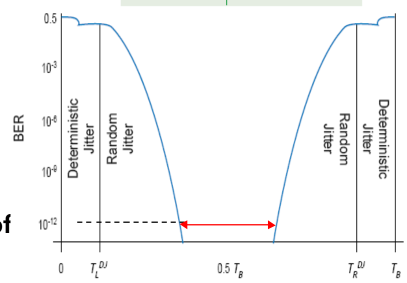


BER	Multiplier
10^{-4}	7.438
10^{-6}	9.507
10^{-7}	10.399
10^{-9}	11.996
10^{-11}	13.412
10^{-12}	14.069
10^{-13}	14.698
10^{-15}	15.883

- **Total Jitter calculation from Dual-Dirac**

$$J_{pp}^{Total} = J_{pp}^{Random} + J_{pp}^{Deterministic} = 14x\sigma + J_{pp}^{Deterministic}$$

- **Convert RMS to Peak-to-Peak for Specific BERs**
- **if 10^{-12} BER is the goal and thus a factor of 14 is used**



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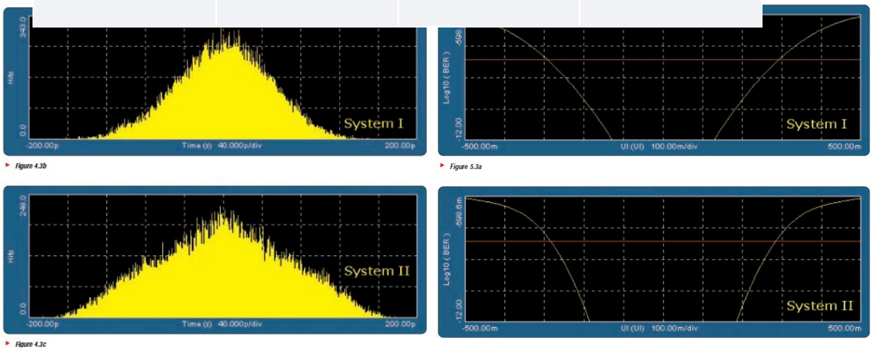
Total Jitter & Bathtub & Jitter Margin

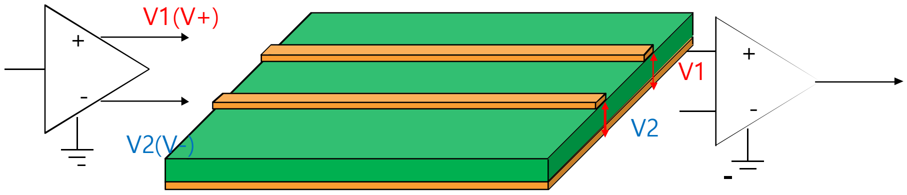
	RJrms	DJ (PJ)	TIE pk-pk
System I	0.053UI	0	0.457UI(430ps)
System II	0.028UI	0.14UI	0.457UI(430ps)

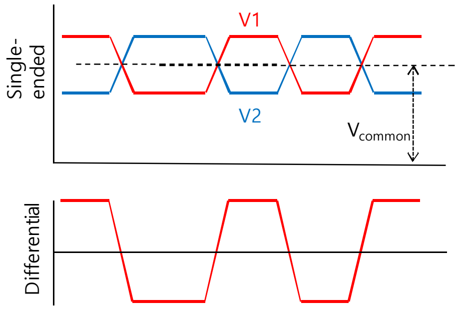
* 10.3125Gbps, Measure 4,000 edges, source: Tektronix



Measurement Setup(Test Points)

Differential Signaling





$V_{differential}$ = V1-V2

V_{common} = (V1+V2) /2

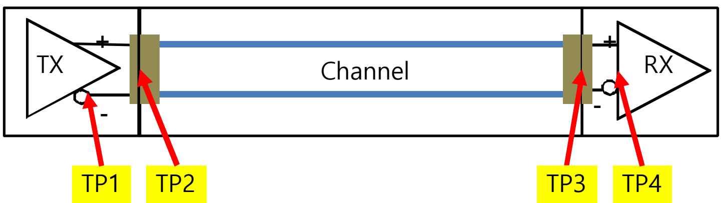
Single-ended V1= $V_{common} + \frac{1}{2}V_{diff}$

Single-ended V2= $V_{common} + \frac{1}{2}V_{diff}$

In AC coupled signal, V_{common} is 0

Test Point Consideration

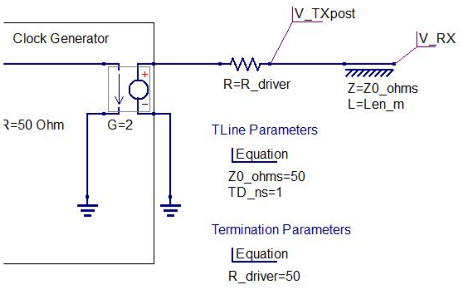
Simplified TX/RX system

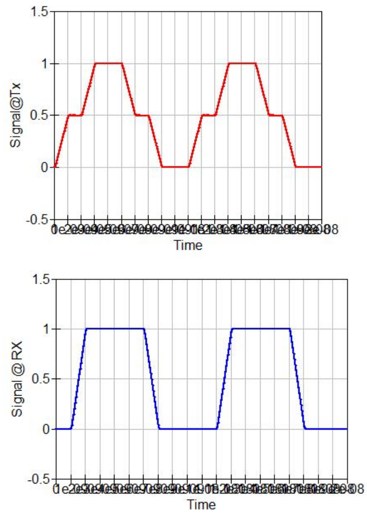


Example of test point(TP)
TP1: Transmitter IC Pin
TP2: Output connector of TX board
TP3: Input connector of RX board
TP4: Receiver IC Pin

Q: What the signal at TP2 shows in this TX+Channel+RX system?

Test Point Consideration

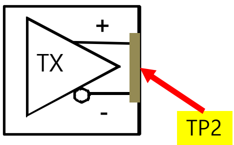




Tx at TP2 and Rx at TP3,
Source Termination

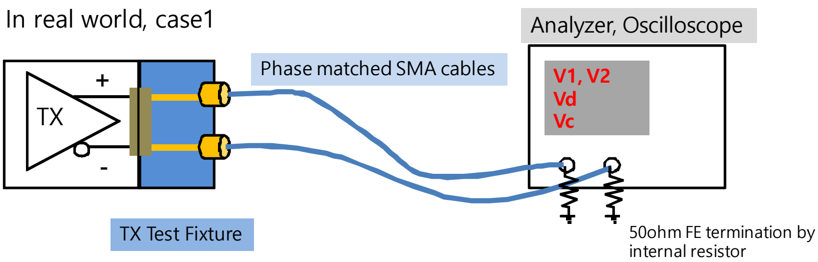
Testing the signal quality of TX

TP2 is typical for TX device testing



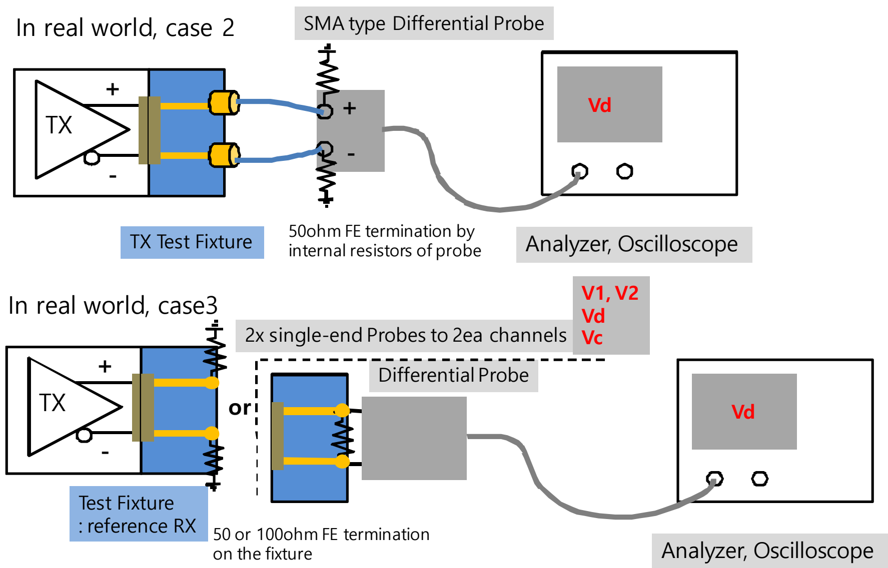
- ✓Jitter
- ✓EYE diagram
- ✓Skew
- ✓Differential waveform
- ✓Common mode waveform(noise)
- ✓Pre/de-emphasis
- ✓SSC

In real world, case1

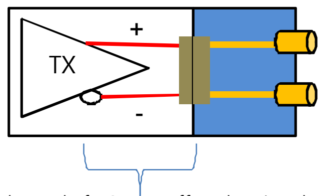


✓Loose(No) coupled differential signaling with Coaxial cables

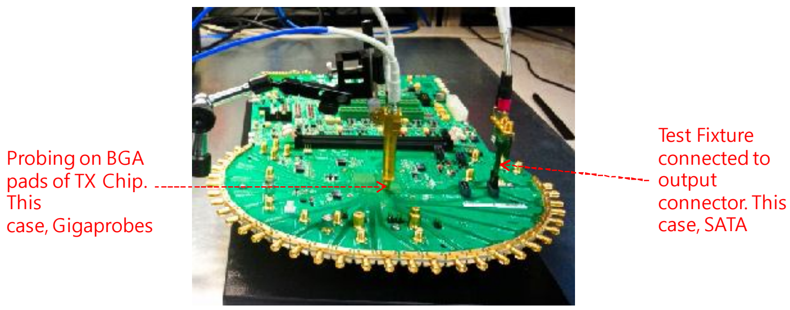
Testing the signal quality of TX



Testing the signal quality of TX

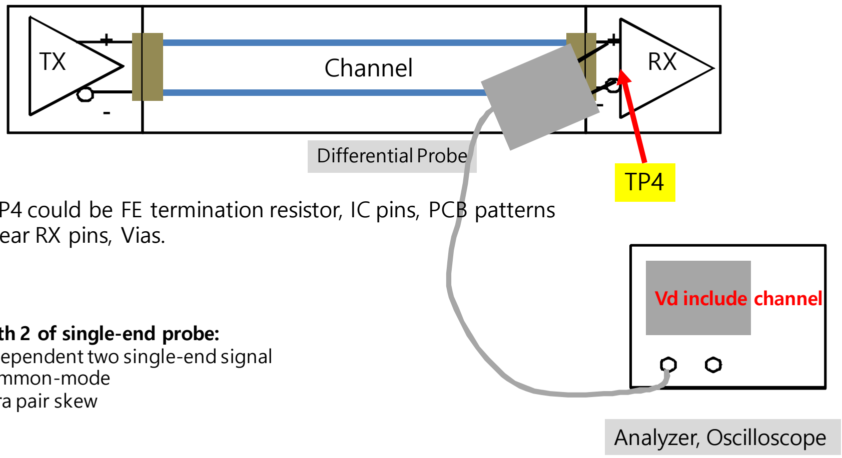


This transmission channel of PCB can affect the signal quality of TX chip.
Test this channel → de-embed this effect from the measurement : S-parameter is used(S2P, S4P)



Testing the TX signal quality at RX

In real world, typical

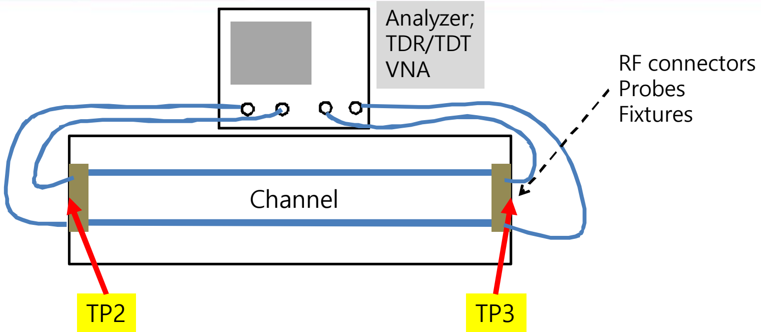


TP4 could be FE termination resistor, IC pins, PCB patterns near RX pins, Vias.

With 2 of single-end probe:
Independent two single-end signal
Common-mode
Intra pair skew

Switchable Multi mode Probe(Differential & Single & Common)

Testing the channel quality

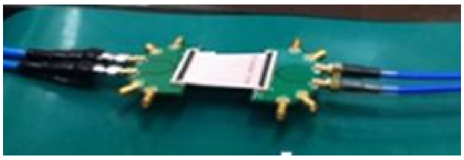


- ✓Characteristic Impedance
- ✓Loss / Reflection in Time domain (TDR, TDT)
- ✓Loss / Reflection in Frequency domain (S-parameter)
- ✓Time Delay and Skew
- ✓Crosstalk
- ✓Mode Conversion
- ✓Waveform/Pulse Response

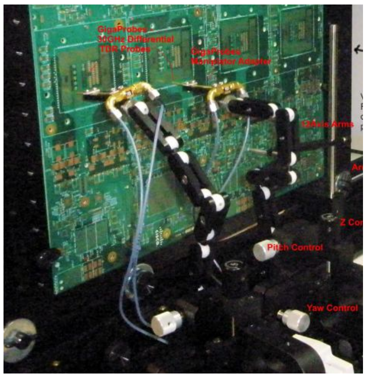
Example of Channel testing setup

Case1, Pad to Connector
Use Probe and Fixture

Case2, Connector to Connector
Use two test Fixtures



Case3, Pad to Pad
Use two probes



Case4, RF connector to RF connector
Use RF connectors

Q & A

Thanks !!!