High Speed and Reliable Gray Mapped Polar Codes

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Abstract— Polar codes have taken a great leap forward in channel coding which has many applications such as fifth generation wireless networks ,robotics and speech converter. When the number of iterations increase, the potential of polar codes is not so striking due to latency and high computation complexity of decoding methods like SCD and BPD. Therefore, based on the idea of gray mapping, we present a pre check scheme with two decoder's namely hard decoder and pure-soft decoder which balance the data reliability and decoding latency. The hard decoder is designed to correct the number of erroneous code words with lesser latency, while the soft decoders aim to correct code words which contain larger amount of errors with long latency. This shows that the polar code concatenated with pre check scheme outperforms the traditional approaches like Turbo codes.

Keywords: *Polar codes, gray map, Error correction code, Pre check scheme*

I. INTRODUCTION

Data transmission has become a vital foundation of our society as effective and more reliable communication services of this ever growing digital world have obtained a significant importance. The amount of data transmitted in the world per second is barely estimable, and it is experiencing an exponential growth. Therefore the capability to transmit fast and reliably has become more and more significant. Channel coding addresses the topic of reliable data transmission. Its purpose is to maximize both the rate at which information is transmitted and its reliability. The revelation of polar codes by Arikan in 2008 [1] spoke to be a noteworthy leap forward in the coding hypothesis. They are the top notch of codes that provably accomplish limit with respect to memory less symmetric channels with low encoding and translating intricacy. Moreover, their express development and recursive structure make them particularly reasonable for quick and productive equipment usage, the colossal intrigue they have stimulated, their useful effect and applications in 5G *[3]* institutionalization as an official channel coding is surprising.

Polar codes soften the wheel to some degree up the field of channel coding. Polar codes work on blocks of images/bits and are in this way in fact individuals from the block code family. The development of these codes take after an extremely unconventional approach contrasted with more customary methodologies like turbo codes proven to achieve the capacity for binary-input symmetric as well as discrete and continuous memory less channels.

Polar codes can be constructed with an efficient encoder and decoder with complexity O (n log n), where n represents the code length. Diverse decoding approaches [3]-[5] for polar codes have been proposed and in those, successive cancellation decoding and belief propagation decoding are the two most popular methods. SCD is serial in nature which suffers from long latency, though it requires less computation.However BPD is parallel in nature, with the increase in number of iterations latency and energy dissipation increases exponentially.

Therefore, the system should be embedded with a appropriate error correction code to guarantee the data integrity and reliability. We proposed the pre-check scheme which is a multi-strategy polar code scheme to strike balance between data reliability and decoding latency. It is embedded with two decoder's namely hard decoder, pure-soft decoders. The hard decoder is mainly designed to correct the more no of erroneous code words unlike the pure-soft decoder to correct code words with larger amount of errors. Also gray mapping scheme is introduced for better error correction performance.

The rest of this paper is organized as follows. Section II gives an overview of polar codes & Existing BPD decoder. Section III introduces pre check mechanism with gray code as mapping scheme. Section IV gives the performance analysis whereas Sect V presents the implementation results. Section VI draws the conclusion.

II. EXISTING METHOD

Polar codes are a linear block code which depends on the phenomenon of channel polarization, where every channel combine and split recursively, such that their mutual data tends toward either 1 or 0. It means, some of these channels become noise-free completely, while rest becomes noisy [3]. Further, the fraction of noiseless channels tends toward the capacity of the underlying binary symmetric channels. Limit accomplishing polar codes have increased noteworthy consideration as of late. Polar codes can be decoded by either successive cancelation or (BP) calculation.

A strategy portrayed known as channel polarization, to develop the arrangements which accomplish the proportionate limit of the double info discrete memory less channel. The proportionate limit is the most astounding one which can be subjected towards utilizing the info with rise to likelihood. This strategy alludes the way that it is conceivable, of autonomous errors.

Polar codes provably accomplish the symmetric limit of a memory less channel while having an unequivocal development [5-7]. The selection of polar codes in any case, has been hampered by the low throughput of their interpreting calculation. This work intends to expand the throughput of polar decoding equipment. These codes are identified by a matrix Gn = $F^{\otimes M}$ where n = 2m is the code length and is the m th Kronecker power of

$$F=\begin{bmatrix}1 & 0\\ 1 & 1\end{bmatrix} \quad (1)$$

Where as

$$G=\begin{pmatrix}1&1&1&1&0&0&0&0\\1&1&0&0&1&1&0&0\\1&0&1&0&1&0&1&0\\1&1&1&1&1&1&1&1\end{pmatrix} \quad (2)$$

An polar code (n,l) is created in two stages. Initially a info v is built by allocating the l dependable and (n−l) untrustworthy locations as data bits and also freeze bits. These (n −l) freeze data are compelled to be 0 and shaped as freeze set AC.

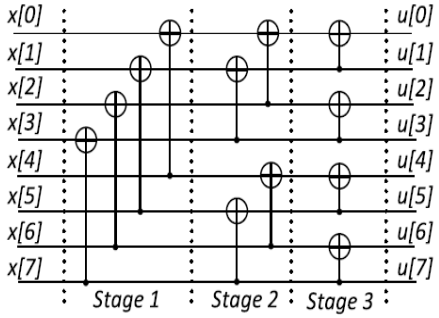

Fig.1 Encoding Flow Graph

Given Rt2m−j a factor graph is arranged j . This got a compact choice lattice ˆx2m−j = [ˆx1 . . . ˆx−j] for these messages, where

$$\hat{\mathbf{x}}2m-j=\begin{cases}\text{`0' if } R2m-j \geq 0\\ \text{`1' if } R2m-j < 0\end{cases} \quad (3)$$

Given ˆx2m−j is an contribution to the factor graph, the decoder data lattice to yield ˆu2m−j, likewise a sub lattice of the origin expression of first polar code, gotten over reverse activity of polar code encoding which is given

$$U_{2(m-j)}^{T}=x_{2(m-j)}^{T}(F^{\otimes(m-j)})^{-1}=x_{2(m-j)}^{T}(F^{\otimes(m-j)}) \quad (4)$$

$$(F^{\otimes(m-j)})^{-1}=(F^{\otimes(m-j)}) \quad (5)$$

The factor graph is freeze if sub origin vector u2m−j fulfils for accompanying solidified rooted benchmark:

$$u_k=0, \text{ for } k \in AC \quad (6)$$

The bits are divided in to information bits and frozen bits and given to encoder and later undergoes polar coding as shown in fig.2. Now we get noisy channel and it is decoded with the belief propagating decoder with a CSFG freezing criterion. Here BPD is parallel in nature so that factor graph is checked every now and then if the processing element is freeze. So that we reduce the area but latency increases with number of iterations.

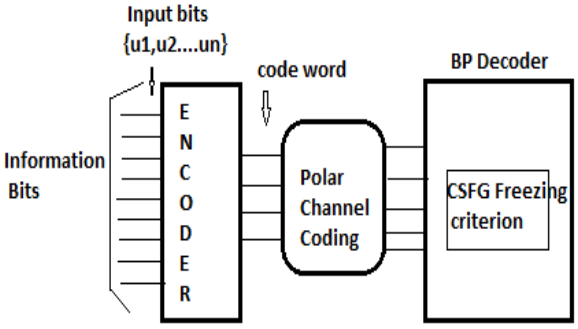

Fig.2 Functional Diagram

In order to implement BP decoding, the authors in [15]-[16] show that the factor graph of these codes can be obtained by adding check nodes to each column of the first n (n = logN) columns from one end to other in the encoding graph. During this process, soft data has updated and propagated among adjacent nodes from the rightmost column to the leftmost one.

An existed Belief Propagating decoding plan depends on a factor graph freezing idea to accomplish bring down multifaceted nature. At a specific emphasis t, if there is factor graph organize j is effectively disentangle to compare essential code, it is freeze and message is not passed or refreshing inside the factor graph is required in following resulting cycles. Points of interest to check if a factor graph is freezing.

It [15] shows that the criteria xˆ HT =0 is satisfied then it undergoes a freezing criterion. However, basing on the analysis and simulation results, the BP decoder will not give a good error-correction performance.

Hence, we consider the following simple but efficient gray mapped pre check scheme.

III PROPOSED METHOD

The information sent will be first processed in the operating system and thereby it is converted in to binary bits and later encoded by polar encoder. Then those bits are consecutively mapped pair wise per cell to be stored. The bits read from the encoder are identified and converted into relating computerized data as per the adopted decoder. There comes the functional diagram of this information storage device. First the data obtained is converted in to binary bits and encoded in polar encoder.

This figure 3 shows the functional diagram of the proposed multi-strategy ECC scheme. The detector will check the cell state to ensure the distortion of the voltage state with the assigned one. Now we can compare and assist which decoder can address the issue easily which is so called a pre check scheme. The pre-check scheme can select an appropriate decoder according to the degree of cell distortion to satisfy performance requirements of the system. After this procedure,

sensed voltages will be processed into different kinds of input information and sent to corresponding decoders.

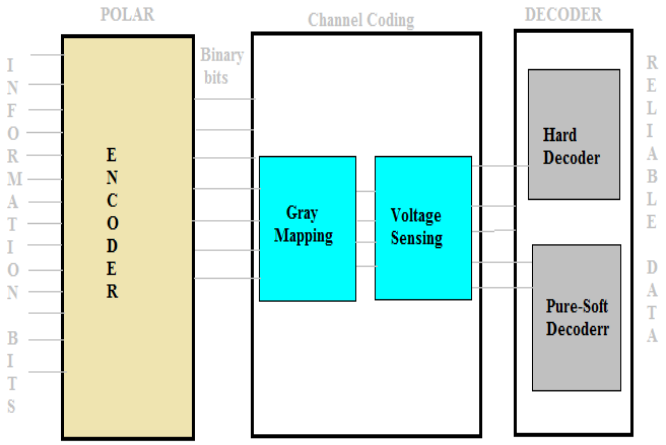

Fig.3 Block Diagram of Proposed System

The hard decoder will be choose if the overlapped regions are small or even nil as its latency considered being short. While pure-soft decoder is choose if the data having much distortion though the its decoding latency is high. Based on the system criteria majority of code words will be decoded in the first decoder itself which in turn improves the overall speed.

Gray Mapping

Now due to its four feasible blend of two bit pairs, the information consists all voltage phases. In the past, direct mapping was the simplest and mostly used associating plan by many academicians. In this plan, the binary structure consists of the those bits matched to voltage phase. It is present in an orderly manner as shown in

Table 1 Encoding Scheme of Four Voltage States

Direct	00	01	10	11
Gray	00	10	11	01

Accounting that, inappropriate bits occur mostly where voltage is consider into its adjacent stages in the finder and other voltage at the centre have two bits contrast. Henceforth, two fold piece errors are happening under the condition that one centre voltage arranged is perceived as another by mess. In this circumstance, we consider map plan which can lessen the quantity of wrong bits are such sort of rough errors. Along these lines, Gray mapping, whose neighboring voltage stages have just single mistake as appeared in Fig.4.5 thereby diminishing the bit-error rate (BER), is clearly our best decision.

Hard Decoder

As aforesaid, we adopted the mapping scheme based on Gray code. Here, we have a modified reading access to generate the sign bits of LLRs needed by decoder. Here the reference V1 is used to distinguish least significant bits (LSBs) of cells. More specifically, as shown in Fig. 4, the received voltage will be compared to V1 to decide if the LSB is 1 or 0.

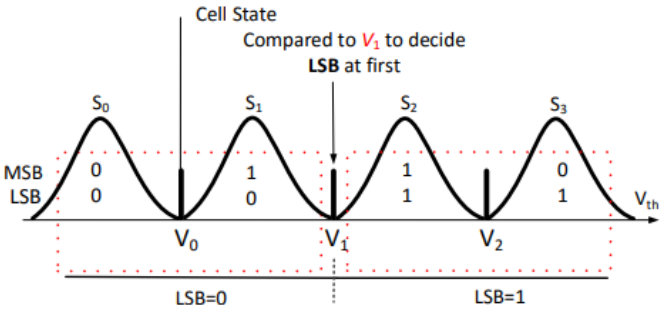

Fig.4 Detecting Scheme for Hard Decoder

When we see that obtained is significant than V1 , then LSB is counted to be 1. The value of MSB is characterized by other reference. After the comparison if LSB found to be '0', then the state is S0 or S1. Hence the value of MSB is determined by V0. Mathematical value can be figure out for these comparisons in this scheme.

Here, each one should be compared 2 times to generate respective data. Therefore, the mathematical expression

$$NM = 1 \mid 4 \times (2 + 2 + 2 + 2) = 2 \qquad (7)$$

Evidently, this plan is the best one as the compared operations in this scheme return 2-bit data, which is the largest amount of data which it can offer. After getting the compared results from detector, hard decoder will generate the sign bit of LLR from these data. These comprehensible LLR can be processed by simpler bit and arithmetic operations in this decoder with lesser no of registers in turn reducing the hardware cost.

Pure soft Decoder

If the data is more distorted when compared to the reference voltage then it is directed here. This will calculate the integrals of particular interval and gets uniformly divided. But we know these do not portray the actual information. Thereby it Vd is the voltage which is considered that every single bit stored in a cell is equally possible either to be 0 or 1, i.e., each bit has same a priori probability of 0.5.Where

$$L(bi) = \log \frac{p(bi = 1|Vd)}{p(bi = 0|Vd)} = \log \frac{p(Vd|bi = 1)}{p(Vd|bi = 0)} \qquad (8)$$

$$L\ (bi) = Log \frac{\sum_{k \in oi} p^{k(Vd)}}{\sum_{k \in zi} p^{k(Vd)}} \qquad (9)$$

Zi and Oi are divergent which depends upon plotting we consider.

IV PERFORMANCE ANALYSIS

The results between existing and pre check scheme are compared and we can clearly see that delay has been reduced from the below figure.

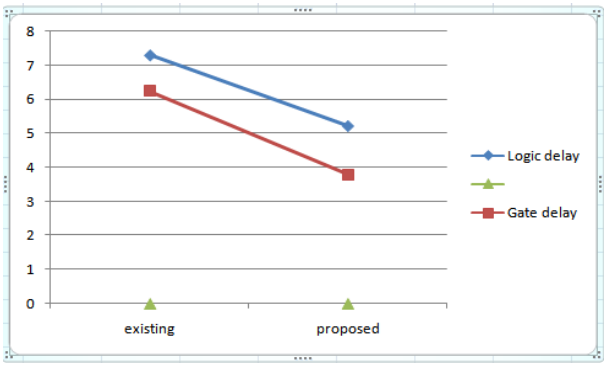

Fig.5 Comparison of delay between existing and proposed scheme

V RESULTS

The performance simulations of gray mapped polar code are carried out in ISIM. Synthesis has been carried out with XA3S500E device of automotive Spartan6 family using Xilinx ISE14.5 tool. The test frequency is 132.258MHz; the power supply voltage is 1.1 V and delay of 8.029ns. The number of slice flip flops are 81, 4 input LUTs 121 and number of 281.

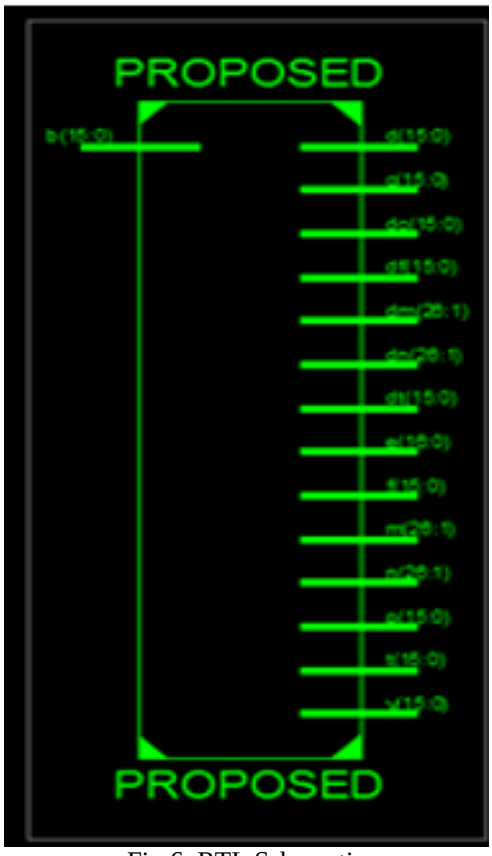

Fig.6: RTL Schematic

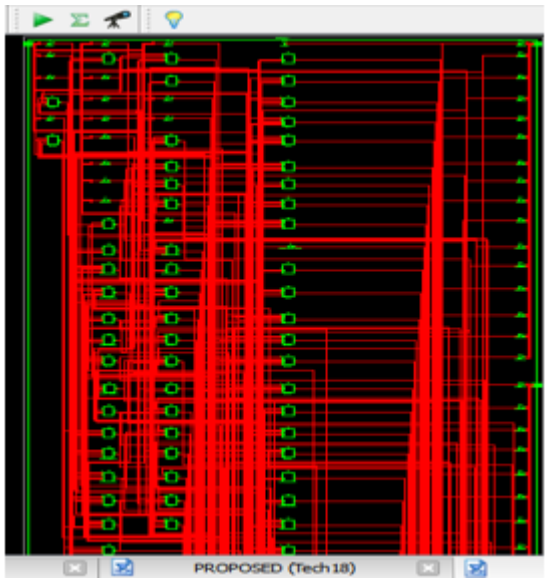

Fig.7: Technology Schematic

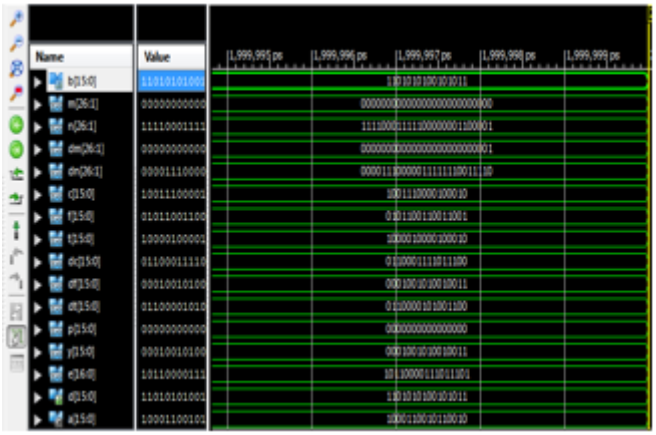

Fig.8: Simulation Result of Pre check Scheme

VI CONCLUSION

Here a polar code with gray plotting is proposed built using pre check scheme which helps to elongate the life time of device with the sensible cost. Hard decoder has a noteworthy role to improve the decoder effectiveness with little bit operations which purely decreases the price. In the interim, the suggested pure soft decoder is impervious to erroneous code words, producing it to make it easier the large-scale application of enterprise-level products. Supplement to it we also prove that Gray code to be the better mapping strategy.

VII. REFERENCES

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