DESIGN AND IMPLEMENTATION OF NOVEL AREA EFFICIENT SCAN BASED LBIST USING LP LFSR

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***Abstract*—** Testing is a fundamental step in Very-Large-Scale Integration (VLSI) design. There are two major steps in VLSI testing. They are Test Generation (TG) and Test Application (TA) . The objective of TG is to produce test patterns for adequate testing and TA is the process of applying those test patterns to the CUT and analyzing the output response. The whole process is performed by LBIST. To handle the rapid increasing complexity of testing, VLSI circuits is to incorporate Logic Built-In Self Test (LBIST) structures. However, LBIST architecture calls for increased area overhead. So it is very important to keep this area overhead to a minimum. And by applying test vectors Power Droop (PD) may appear in LBIST which will generate a delay affect on the circuit under test (CUT) and it is recognized as a fault. So here in this paper, we designed a novel area efficient scan-based LBIST, and it is achieved by using the LP-LFSR and also by proper modification of test vectors. As a result, 72.5% of area and power droop of proposed system is diminished than the existing method and by SA high fault coverage is also achieved. The proposed design architecture has been coded in VERILOG HDL and the software used is Xilinx 13.2.

Keywords*—VLSI, LP LFSR, Power droop (PD), LBIST, CUT, Test Generation, Test Application, SA.*

I. INTRODUCTION

LBIST stands for Logic Built-In-Self-Test. now-a-days logic blocks at-speed test are performed by using LBIST (LBIST). It depends on the CUT which is either a sequential circuit or combinational circuit [8], [12]. It is achieving importance by providing oneself test ability to logic thus, the IC can check itself which completely diminishes the use of external equipment & also by finding faults in a circuit design reduces the difficulty in VLSI testing.

There are two primordial capture-clocking methods in scan based LBIST. They are: 1) the skewed-load (also called as launch-on-shift (LOS)) method and 2) the board-side (also called as launch-on-capture (LOC)) method.

In skewed-load method, Test Vectors are employed at the prior clock of the expedient period in the circuit under test and at the following seized the outputs from CUT are studied on the scan chains.

In the board-side method, during the expedient period, TV are initially fed into the scan chains(SC); then, in seized period, TV are applied to the CUT, and the CUT output is indentured on scan chains.

It experiences a Power Droop (PD) challenges, because of high Activity Factor which is caused by the application of test patterns. Particularly through the capture phase..

The increase in power droop (PD) and area are major concerns for ICs' testing. Excessive power droop (PD) will lead to IC fail, due to the abrupt changes in circuit activity (CA). So there is need to reduce the excessive pd and area.

In this paper, TG is done by using LP-LFSR which generates the test vectors to diminish the circuit activity and switching activities of the CUT.

II. LITERATURE REVIEW

"Low power BIST for scan-shift and capture power" Proposed by Y. Sato, S. Wang, T. Kato, K. Miyase, and S. Kajihara, in Nov.2012[2] presents a paper which had been examined greatly to attain precise and systematic testing. However, there are numerous enlightened approaches for scan-test, but there are less for LBIST due to its unmanageable randomness. Although, LBIST presently becomes more essential for design amend. Authors designed a new LP BIST technology which decreases shift-power by preventing the prescribed uplifted frequentness partly vectors and also decreases the capture power. The authors demonstrates the proposed technology not only reduces test power but also keeps test coverage with less loss.

"A low power pseudorandom BIST technique", Proposed by N. Z. Basturkmen, S. M. Reddy, and I. Pomeranz, in Jul.2002[9], suggests a new pseudo-random BIST method for scan designs, which is utilized to decrease the consumption of peak power. This approach decreases the switching activity in both the scan chains and circuit under test by limitation of scan shifts to a part of the scan chain configuration using attenuation of scan chain. On different benchmark's circumambulate showed that this decreases the switching activity. The authors demonstrates that their paper will surely decreases the switching activity which are produced by scan shifts.

"Automated synthesis of large phase shifters for built-in self-test,"Proposed by J. Rajski, N. Tamarapalli, and J. Tyszer, in Oct. 1998[10] -This proposes a novel method for the self-operating synthesis of phase shifters – here components are

used to shed affects of structural reciprocity signed by 2-d test generators. The algorithms proposed in this paper synthesize in a time-ultra efficient form super fast phase shifters for bist environment, with promised minor phase shifts between scan chains, and less delay and size of partly one two-way exclusive or gate per channel.

III. PRIOR WORK

In this work, PRPG block is implemented by using LFSR and the non-storage elements in the CUT are changed into many Scan flip-flops.

The widely used scan-based LBIST architecture is adapted and presented in Fig.1.

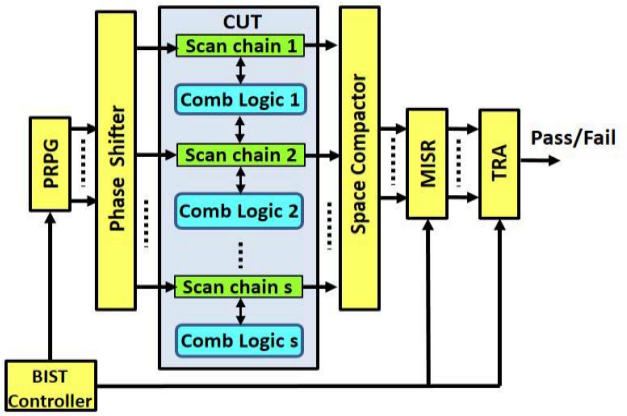


Fig.1.Block Diagram of the adapted Scan Based Logic BIST architecture.

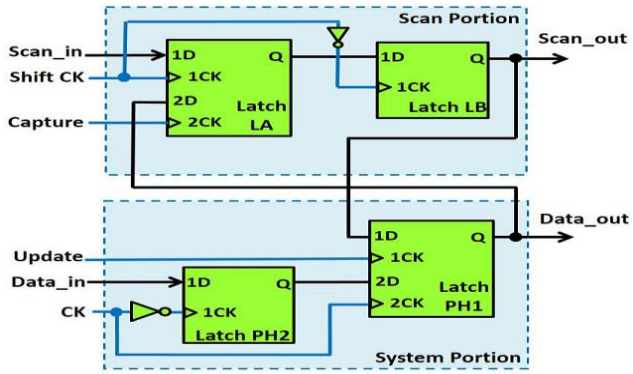


Fig. 2. Internal diagram of SFF

Flip-Flops in Scan chain(SC) are known as scan FFs, as for SFFs this work needs that, through expedient period, they preserve the prior TV which are fed to the CUT. It is authenticated by the SFF in [24].

In Fig.2 the internal diagram of SFF's is shown. There are 2 sub blocks, named as, the system portion and the scan portion. They comprises of a Master-Slave FF's tranquilized of 2 latches (one is for the system portion, and another is for the scan portion) [24]. In Fig. 2. The method of clocking considered a broad side method which consists of a expedient phase and a seized phase.

The aim of the method is to diminish the Power Droop (pd) at speed test which will produce the faults in SB Logic Built In Self Test. Power droop problems rises when a substitute test vector (STV) are fed to the CUT.

This is shown at the Update pulse in Fig. 3. through seized phases. The obtained power droop is directly proportionate to the Activity Factor of CUT.

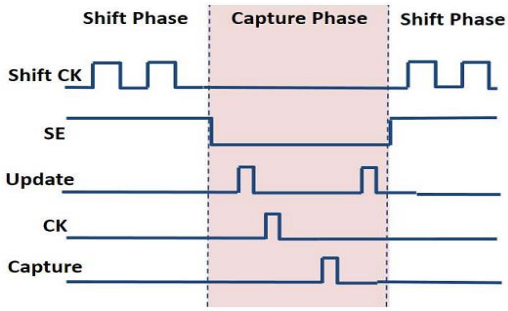


Fig.3. Clock Waveforms for internal structure of SFF's

In existing method a mathematical description is derived, by considering the two rules for Conventional LBIST.

1) Every SC should have the similar number of SFF's.
2) The highest Activity Factor between two test vectors T_i^m and T_{i+1}^m which are similar for every SC (m = 1 ... s).

In this method, the STV ST_i^m is asserted in the Scan Chain m ,at the ith seized period it is appealed to Circuit Under Test based on the TV T_{i-1}^m and T_{i+1}^m which are applied at the seized period (i − 1)th and (i + 1)th respectively.

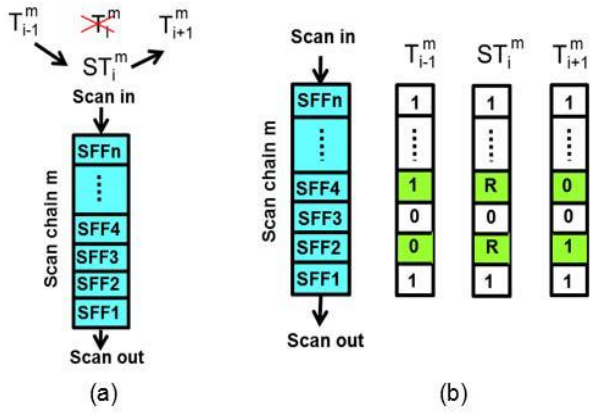


Fig. 4.(a) Order of TV filling each and every SC m,
(b) Bits in the STV ST_i^m and in the TV fed at the last/subsequent seized period (T_{i-1}^m/T_{i+1}^m).

Signifying by ST_i^m (j) , T_{i-1}^m(j) ,and T_{i+1}^m(j) the value of the j th bit in TV ST_i^m , T_{i+1}^m *and* T_{i-1}^m respectively, ST_i^m (j) is preferred as below,

$$ST_i^m(j) = \begin{cases} T_{i-1}^m(j), & If\ T_{i-1}^m(j) = T_{i+1}^m \\ R\ , & If\ T_{i-1}^m(j) \neq T_{i+1}^m \end{cases}$$

Here R is a random bit.

Consequently, in all bit positions j where TV $T_{i-1}^m$and T_{i+1}^m varies , and ST_i^m presumes a R value . The R bit may solely came from the outputs of LFSR.
Beginning from the (i − 1) th seized period (Fig. 3), the STV sequence in each scan chain m will be as follows :

$$T_{i-1}^m - ST_i^m - T_{i+1}^m - ST_{i+2}^m - T_{i+3}^m \ldots\ldots$$

Consequently, the no. of bits are altering their rationale value among the next TV with the novel order $T_{i-1}^m - ST_i^m - T_{i+1}^m$ and that will be same, or lesser than, those with the earliest TV order $T_{i-1}^m - T_i^m - T_{i+1}^m$ of Conventional LBIST.

The R in ST_i^m in the positions where T_{i-1}^m and T_{i+1}^m vary permits a novel order $T_{i-1}^m - ST_i^m - T_{i+1}^m$ to maintain the erratic nature of the actual order. Consequently, the no. of TV involved to attain a better fault range are not raised differentiated with the usage of the actual order. The extreme CF among the successive TV are fed in each and every scan chain in Conventional LBIST (CF_{con}^{SC}) is decreased to a partly($CF_{con}^{SC}/2$) by this method. Therefore, signifying by CF_{ST}^{tot} the extreme AF among any 2 following TV are appealed to CUT at following seized period, for this method with STV, is written as below,

$$CF_{ST}^{tot} = AF_{con}^{tot}/2$$

Where CF_{ST}^{tot} is the max CF obtained.

To implement, the existence of a Phase Shifter strengthens the CUT. Denoting by O^m (m = 1 ...s) , in j th place of the I th TV of the SC m the logic value T_i^m(j) is written as

$$T_i^m(j) = O^m(\xi) \quad (1)$$

where ξ = n(i − 1) + j is the overall no. of expedient CKs from the starting of the test.

In this manner , the values are charged in the jth place of Scan Chain m in the expedient period prior the (i-1)th, the i, and the (i + 1)th seized period are well matched to value instant at the result $O^m$of Phase Shifter, follows ξ − n, ξ, and ξ + n expedient CKs, calculated from starting of the check. So, we can demonstrates the values instant in the jth place of the prior and the succeeded TV T_{i+1}^m (j) and T_{i-1}^m(j), for each and every SC m and seized period i are given as,

$$T_{i+1}^m(j) = O^m(\xi + n);\ T_{i-1}^m(j) = O^m(\xi - n). \quad (2)$$

Therefore the Phase Shifter permits to its results several prior/upcoming values of each and every O^m.Consequently, two PS outputs $O^k$and O^p are occurred with k = p = m, they are as follows,

$$O^m(\xi - n) = O^k(\xi); \quad O^m(\xi + n) = O^P(\xi). \quad (3)$$

The equations in (2) and (3) are used in deriving a existing method.

In Fig.5(a) a Design and implementation of the existing method is shown.

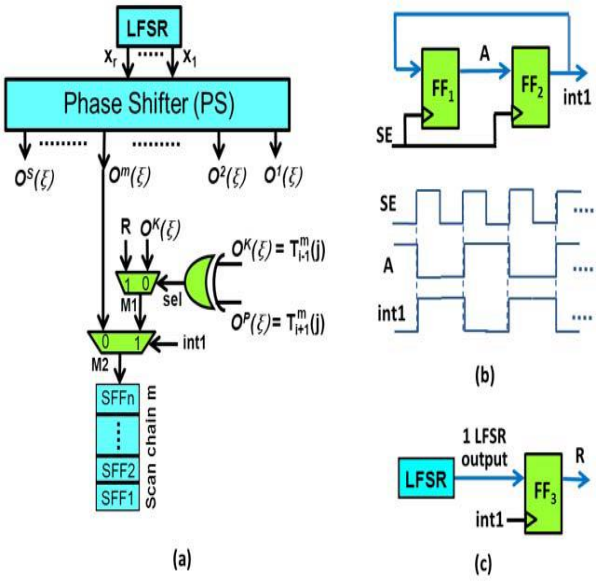


Fig. 5. (a) Design and implementation of the existing method (b) approach to produce signal *int*, and (c) Shows scheme to produce R.

This method involves multiplexers and an exclusive OR gate. Multiplexer M2 permits us to arms the succeeding in the SC m:

1) The TV $T_{i-1}^m$and T_{i+1}^m produced by the Phase Shifter through the expedient period prior the (i −1)th and (i +1)th seized series, by mounting int1 equal to 0;
2) The STV ST_i^m provided by multiplexer M1 through the expedient period prior the ith seized period, by mounting int1 equal to 1. Especially, the signal int1 is produced in a manner that it handles the values from 0 to 1 and 1 to 0 at the succeeding seized period.

In Fig. 5(b). int1 generation is depicted. At first, set FF2 to 0 and FF1 to 1. FF2 and FF1 are recorded by the Scan Enable (SE). So, rising edge, int1 handles the values from 0 to 1 at intervals of Scan Enable . The Exclusive OR gate is utilized to compare the value at the result of Phase Shifter $O^k(\xi)$ [=T_{i-1}^m(j)] to the value at the result Phase Shifter $O^p(\xi)$ [= T_{i+1}^m(j)] at each and every expedient CK j. Finally, the random bit R is easily produced from any output of the LFSR. So in this method they uses the similar R value for the entire expedient period.

And in Fig. 5(c) a realizable scheme is shown to produce the Random bit R. LFSR results are charged into an Flip-Flop (FF3), which is recorded by int1 signal. Flip-Flop 3 is sampled

on R a novel value instant at the each rising edge of int1 and a3t result of LFSR, and it maintains it until the succeeding *int1* raising edge. In this manner, the similar *R* value is utilized through a entire expedient period.
In this scheme, *R* outcomes in a highly unequal no. of zeros or ones in each and every Substitute Test Vector, and depends on *R* value either 1 or 0.

IV. PROPOSED METHOD

In the proposed method, LP-LFSR is used in the place of normal LFSR to reduce the area of the LOGIC BIST based architecture which resulted in high fault coverage. Hence the area of the scan based Logic BIST is diminished. A Scan-Based LBIST architecture using LP-LFSR is as shown in fig.6.

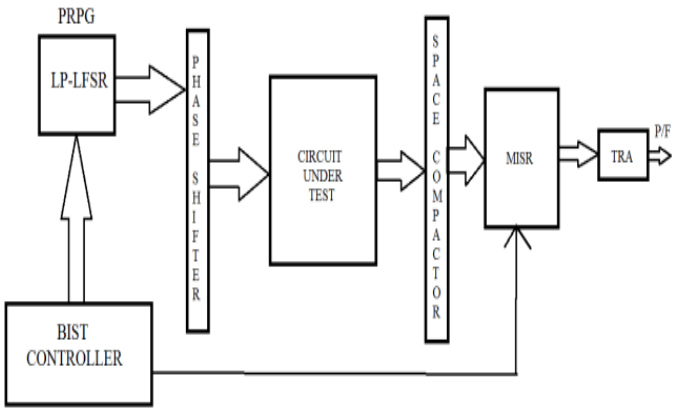


Fig.6. Architecture of PROPOSED SYSTEM

A block diagram of proposed system consists of SEVEN Blocks. They are:
1. BIST CONTROLLER (BC)
It is used to provide all necessary inputs to initialize each and every blocks. It commands the operation of the LBIST, they are initialization, propagation of clock, and scan chains flow in and out .

2. PSEUDO RANDOM PATTERN GENERATOR:
Vector from BC is used to initialize the PRPG block. In this method, PRPG is implemented by using LP-LFSR. Here it generates the pseudo random sequences which are fed to the CUT to be tested.
LP-LFSR:
Low Power LFSR [LP-LFSR] is utilized to produce test patterns. Here a new design is determined to produce the test patterns with diminished switching activities.
3. PHASE SHIFTER (PS):
The Phase Shifter (PS)[10] is utilized to expedient and seized the TV which are produced by PRPG. At the similar clock cycle, the Phase Shifter gives a results, the instant LP- LFSR sequence together with numerous prior/next sequences. It permits us to diminish the connection among the TV connected to SC's.

4. CIRCUIT UNDER TEST (CUT):
It is the major block where testing customarily resides of interrelating set of test stimuli (input patterns and test vectors) and it consists of scan chains and combinational logic.

5. SPACE COMPACTOR (SC):
A Space Compactor is widely adopted to compact the outputs of the CUT to test yields.

6. MULTIPLE INPUT SIGNATURE REGISTER (MISR) :
MISR produces packed result that is contrasted and utilizes a comparator to test where the circuit is defective or fault free circuit.

7. TRUE RESPONSE ANALYZER (TRA) :
TRA is the output of the circuit which is used to determine the definiteness of the CUT. If TRA matches output is zero(pass) else 0 (fail).

V. PERFORMANCE ANALYSIS

Compared to using normal LFSR, by using LP-LFSR in proposed method the area is reduced compared to the existing system is shown in table 1, the area is decreased by 72.5%.

S.NO.	LOGIC UTILIZATION	NORMAL LFSR	LP-LFSR
1.	NUMBER OF SLICES	54	42
2.	NUMBER OF FLIP-FLOPS	80	58
3.	NUMBER OF 4-LUTs	35	35

AREA ESTIMATED GRAPH

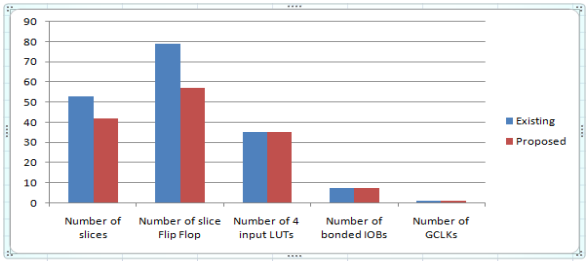
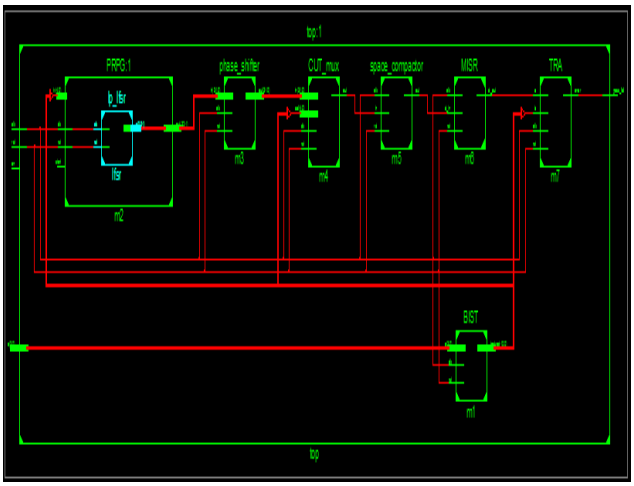


Fig.7. Overall Comparison of AREA between Prior and Proposed work

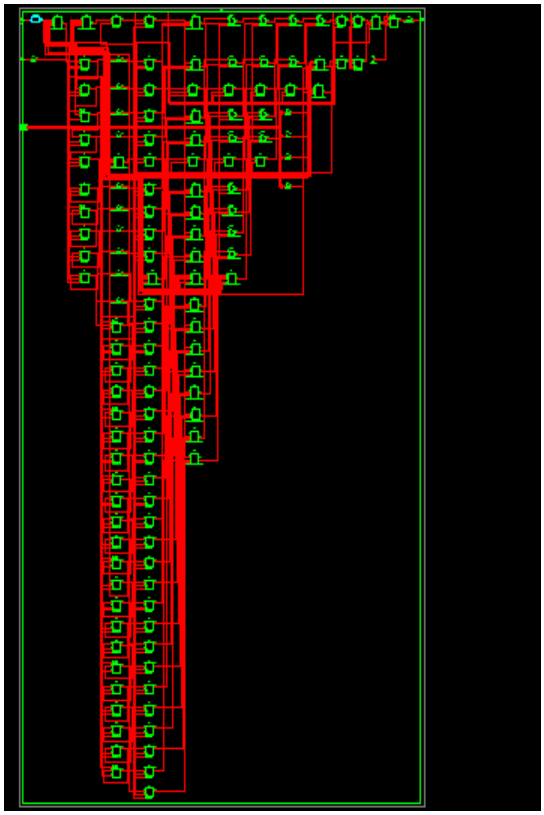
VI. RESULTS

Different blocks of proposed system are coded in VERILOG HDL, and Xilinx ISE is the firmware apparatus used for FPGA synthesis.

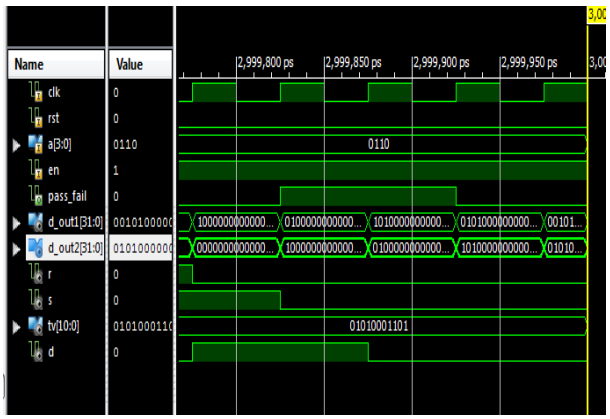
RTL SCHEMATIC



TECHNOLOGY SCHEMATIC



SIMULATION RESULT



VII. CONCLUSION

In this paper a NOVEL AREA EFFICIENT LOGIC BUILT IN SELF TEST architecture where each and every component is implemented and simulated using Xilinx 13.2.software and I Simulator. The Scan Based LBIST circuit is designed using LP- LFSR. Proposed architecture gives better performance than the existing method by 72.5% area reduced. And with the presence of MISR, High Fault Coverage is also achieved.

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