Fault Tolerant Soft Processor on FPGA

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***Abstract*—** This paper presents mechanism to design and implement soft processor on FPGAs. Error-correcting code technique is used, which harden the fault tolerance of soft processors. FPGAs suffer from highly susceptible radiation induced faults example Single Error Upsets. Memories of FPGAs are more susceptible to these faults. Error-correcting code technique is demonstrated in implementation of a fault tolerant soft processor on Xilinx FPGAs. In additional we used LookAhead technique to synchronize Error-correcting code-protected Block Read Access Memory (ECC BRAM) with the soft processor. The resulting fault tolerant soft processor has benefit to self recover the program memory in presence of Single Error Upsets, without halting the processor.

Keywords*—Fault tolerance,Field Programmable Gate Array(FPGA),SEU.*

I. INTRODUCTION

Due to complex architecture and reconfigurability feature of Field Programmable Gate Arrays (FPGAs) have brought advantages to many applications such has safety critical aerospace and mission critical applications. Functionality of FPGAs can be further enhanced either in the form of built in hard cores or soft cores. Example of hard core is PowerPC on Xilinx FPGAs and examples of soft cores are PicoBlaze and MicroBlaze from Xilinx and Nios from Altera. Due to flexibility and compatibility with high level applications this soft core processors has increased uptake in many applications. The most commercial FPGAs, which are SRAM based FPGAs suffer from radiation induced faults e.g. Single-Error Upsets (SEUs). These faults are provoked in space by high energy particles. Due to Single-Error Upsets (SEUs) faults, FPGAs memory cells are hardened to be robust than traditional SRAMs. FPGAs memory cells are hardened for fault-critical applications example in space [1]. Block memory (BRAM) is manufactured with small cells which contain more data so they are still unprotected.

Block memory (BRAM) is used by most FPGA soft processors to store program and data memory. BRAM require more attention when used in safety critical applications. Built-in Error Correcting Code (ECC) circuitry is developed by Xilinx for their BRAMs [2]. ECC circuitry can automatically correct single bit error and detect double bit errors. Fault tolerant versions of soft processors needs to be synchronized with ECC mechanism. Soft processor typically needs memories with one clock cycle whereas BRAM of ECC requires two clock cycles. To solve the synchronization problem ECC Processor Adaptor (EPA) is used, which solves problem by looking ahead the next instruction. This is demonstrated in design and implementation of a fault tolerant soft processor.

II. BACKGROUND STUDY

Previously, a Fault Tolerant version of open source LEON-3 FT was proposed [3]. European Space Agency, ESA, in late 1997 initiated LEON project to study and develop a high-performance processor to be used in European space projects. Based on a 5-stage pipeline all LEON are implemented. Errors are detected and corrected by LEON which is caused by SEU's in processing unit. LEON however consumes more resources.

Roll Forward Error Recovery technique is used by Fault Tolerant Soft core processors which uses Triple Modular Redundancy (TMR) to correct error [4]. Triple Modular Redundancy (TMR) is simple and practical. It triplicates functioning modules and if any one module fails majority voter is used. But it consumes more hardware resources which limits the possibility of building more powerful system [5].

III. FAULT TOLERENCE

Fault tolerance is property that enables system to continue its operation even if one or more components fail. Fault tolerant design can reduce the maintenance cost as failure of system reduces [6].

Fault tolerant can be expressed in two ways i.e. reliability and availability. Reliability is that a system will remain operational despite of failure for duration of a mission. High reliability is most important in application in which failure could mean loss of life e.g. critical applications such as space

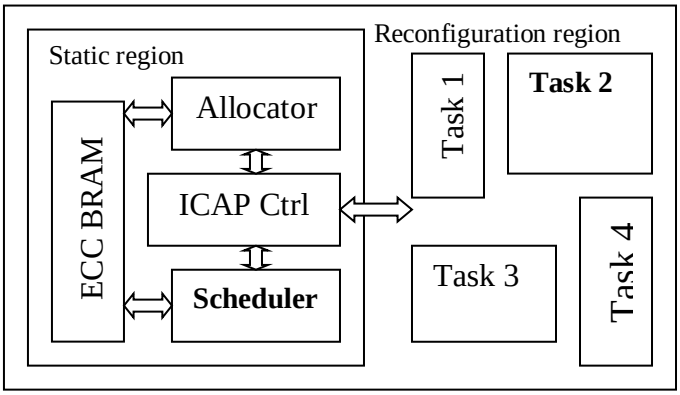

Fig.1: Overall system architecture

shuttle or industrial control. Availability is fraction of time system is operational. High availability is important in applications where every minute of downtime translates into revenue loss e.g. airline reservation and telephone switching.

IV. OVERALL SYSTEM ARCHITECTURE

In FPGA devices, at runtime faulty bits in configuration memory can be reconfigured [7]. This dynamic reconfiguration can bring practical solution. Dynamic reconfiguration is made through internal configuration access port (ICAP) internally with no need of external monitoring circuitry [8]. FPGA can be continually supervised by reading back the configuration memory periodically.

In overall system architecture, FPGA chip is divided into two regions: reconfigurable region and static region (Fig 1). Hardware tasks can be swapped in/out in reconfiguration region whereas main system is located in static region. Fixing emerging faults through scrubbing or reallocating task away from damaged resources is used for achieving fault tolerance in reconfiguration region. ECC BRAM is used to protect system in static region.

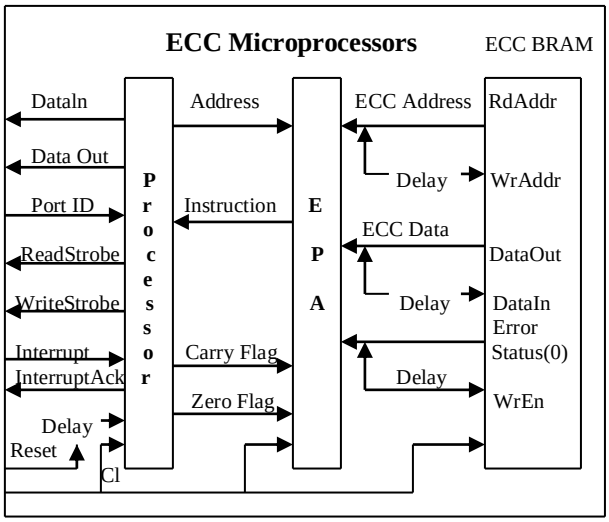

Fig.2: ECC Microprocessor

Three kernel processors exist in static region: task allocator, task scheduler and ICAP controller. In task allocator, hardware task can be allocated and in task scheduler hardware task can be scheduled. In ICAP (internal configuration access port), hardware task can be configured in real time [9] [10].

V. ECC MICROPROCESSOR

ECC microprocessor consists of three main blocks: processor, EPA (ECC Processor Adaptor) and ECC BRAM figure 2. We will start with processor and ECC BRAM brief introduction. And then present EPA integration with processor and ECC BRAM.

A. Processor

Processor used is 32 bit Xilinx soft-core processor. In BRAM, program memory is implemented. Processor requires 2 clock cycles for each operation including fetching, decoding and executing. Processor fetching requires one clock cycle latency.

B. ECC BRAM

ECC BRAM is combination of two BRAM blocks. Error correction coder/decoder is added to BRAM blocks. Detection of double error and correction of single error is possible with error correction coder/decoder. BRAM can store 1024 18 bit instructions. ECC BRAM has two clock cycle latency, which is not compatible with processor fetching.

C. ECC Processor Adaptor

ECC BRAM and processor are interfaced using ECC Processor Adaptor (EPA). EPA can fetch next instruction which resolves the problem of reading data delay from the ECC BRAM..Figure 2 shows interface between ECC BRAM and processor which is interfaced using EPA. Same memory address is used in ECC BRAM to save two consecutive instructions. Least Significant Bit (LSB) of processor address is used to select instruction between two fetch instructions. LSB of processor address is not been sent to the ECC BRAM.

VI. SELF RECOVERY ABILITY

The memory remains uncorrected while automatically read out data is corrected. As memory is not corrected, the logic is implemented to write back to memory. 2 bit error status output is used to implement logic. When error bit is 00 then it indicate no error, while when error bit is 01 then it indicate single error, when error bit is 10 then it indicate double error and when error bit is 11 then it indicate undefined error. To enable one write back WE port is connected to first bit of 2 bit error status output. To enable WE port status is 0 of first bit of error bit output. Address of the writing back is delayed by four cycles to avoid collision of read operation and write operation. System needs to be scrubbed when status bit is one i.e. uncorrected error.

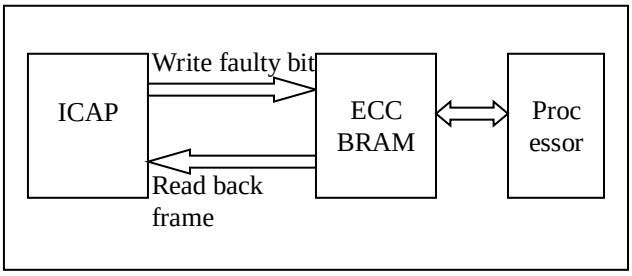

Fig.3: ECC BRAM fault injection

VII. IMPLEMENTATION AND TESTING

A. *Testing*

In task scheduler and also in task allocator ECC protected processor is used in which EDF and BF-EAC algorithms are implemented. All instruction sets of soft processor are covered and tested in both algorithms as they deal with matrix computation and extremely high iterations. Output shows that functionality of ECC processor is same as regular soft processor, but drawback is of 10% speed loss.

B. *Verification*

ICAP (internal configuration access port) is used for injecting faulty bits in the ECC BRAM for verification of the self recovery ability (as shown in figure 3). Experiment shows that single bit is detected and corrected while double bit is detected.

VIII. CONCLUSION

In this paper, we presented architecture of fault tolerant soft processor on FPGA, in which we used Error correcting code program memory. Due to this we can use ECC BRAM as program memory, by this Single Error Upsets (SEUs) can be detected and corrected in processor program memory. ECC processor adaptor (EPA) is developed to achieve this, where EPA synchronizes ECC BRAM read and instruction fetching of processor. Single bit error can be fixed in ECC BRAM using self recovery architecture which we designed. This architecture works without affecting execution of processor.

These can be further improvised to porting with other FPGA soft processors.

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