Comparative Study and Designing of Look Ahead Carry Adder and Ripple Carry Adder

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Abstract- The difference between look ahead carry adder and ripple carry adder is proposed in this paper. Both these adders have been designed using a VHDL (very high speed integrated circuit hardware description language) tool named Xilinx ISE Design Suite 12.4_1. In VHDL tool, structural modeling is implemented on the above mentioned adders. This paper is focusing on difference between these adders based on their performance (fastness).

Keywords- *LCA, RCA, VHDL, Xilinx ISE Design Suite.*

I. INTRODUCTION

There are two types of adders which are going to be explained in this paper viz. Ripple carry adder (RCA) and Look ahead carry adder (LCA). These both kinds of adders are used for adding purpose. In this paper, both adders are designed for 4-bit addition operation. Ripple carry adder sometimes also called as parallel adder because it is used to add a group of bits. Ripple carry adder is required some full adders and one half adder to perform addition operation. This one half adder can be replaced by a full adder also. Finally, ripple carry adder can be designed by full adders for n-bit parallel addition. Ripple carry adder can be designed by using half adders only with some extra or gates. In RCA, carry is generated serially [1]. Look ahead carry adder does the same as RCA. Look ahead carry adder has a carry generator network. Carry generator network is known as look ahead carry network. This carry generator network is used to generate carry. LCA is the fastest adder then RCA, because carry is generated in parallel using 2-level AND-OR look ahead carry network.

II. ADDER STRUCTURE

The structures of both adders are described below:

A. Ripple carry adder

A ripple carry adder uses (n-1) full adder and 1 half adder to perform n-bit addition operation. The half adder is used to perform least significant bits (LSB) addition. This one half adder can be replaced by a full adder. To design n-bit RCA using full adder only n-full adders are required. Ripple carry adder can be designed by using half adders only. To design n-bit RCA, (2n-1) half adder with (n-1) extra or fate is required [2].

1) Structure of a 4-bit ripple carry adder

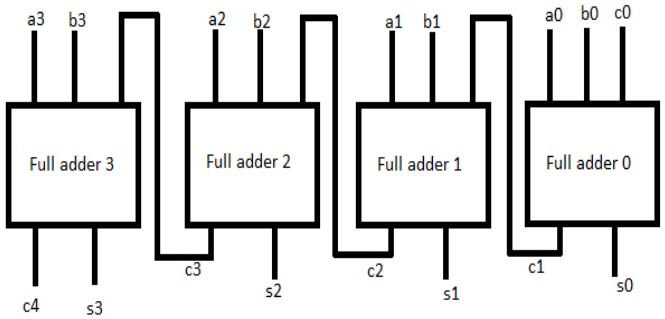

Figure 1: Ripple carry adder using full adder

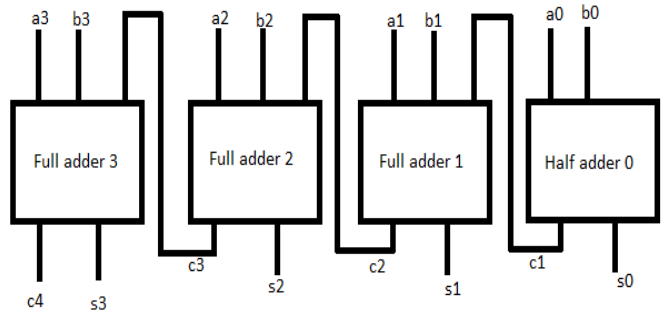

Figure 2: RCA using full adder with one half adder

Fig.1: represents 4-bit ripple carry adder structure using full adder. A 4-bit RCA required four full adders to perform 4-bit addition operation. In this structure, LSB's of two numbers a0 and b0 are producing sum LSB bit. Carry of these LSB bits is propagates to the next bit addition. One extra bit c0 (i.e. initially zero) is applied to the third input of full adder. Carry

of each bits in RCA propagates to the next bit as the manner as c1 (carry is generated by LSB's addition) [3]. Fig. 2: represents 4-bit RCA structure using full and half adders. Third bit of LSB's full adder is zero as shown in Fig.1. So this LSB full adder can be replaced by a half adder. A 4-bit RCA required [(4-1=3)] full adders with one half adder. In above both structures of RCA, carry is propagating from LSB to MSB bits. Ripple carry adder can be designed using half adders only. One full adder can be replaced by two half adder and one or gate. So RCA has [((2*4)-1) =7] half adders with [(4-1) =3] or gates.

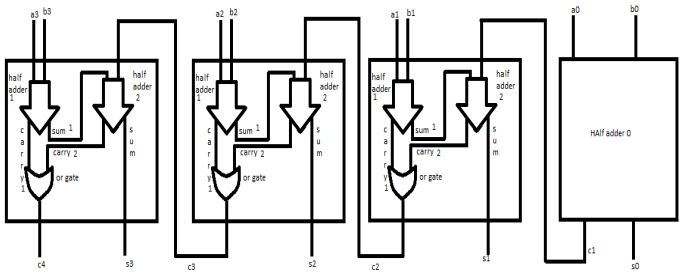

Figure 3: RCA using half adders

B. Look ahead carry adder

Look ahead carry adder circuit diagram is shown in below figure.

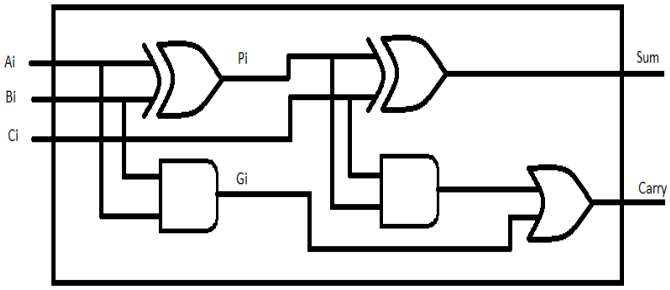

Figure 4(a): LCA circuit diagram

In fig.4(a): Ai, Bi, Ci are the input bits. Pi, Gi is repersented as carry propagation term and carry generator term respectivily. Sum and carry are the outputs of look ahead carry adder [4].

Fig.4(b): repersents 4-bit look ahead carry adder's structure. LCA consists of look ahead carry network.

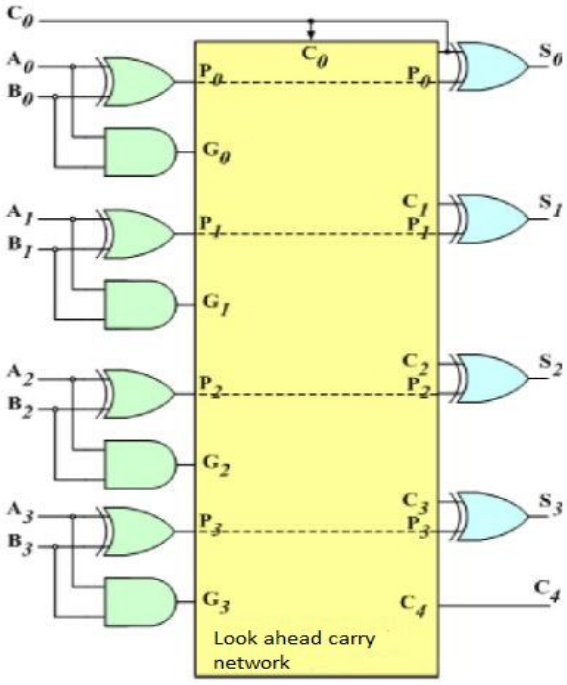

Figure 4(b): 4-bit LCA adder

This look ahead carry networkis responsible to generate carry in parallel way. Look ahead carry network is 2 level AND-OR network. An n-bits look ahead carry adder require [(n(n+1))/2] no. of AND gates, and n no. of OR gates.SO a 4-bit look carry adder is required [(4(4+1))/2=10] AND gates, and 4 OR gates.

III. DESIGN AND SIMULATIONS

Design and simulation of both the adders is done by using Xilinx ISE Design Suite 12.4_1 tool. Look ahead carry adder is designed with data flow style of modelling, whereas ripple carry adder is designed with structural style of modelling in VHDL. In VHDL, data flow style of modelling uses the concurrent Boolean statements to design a circuit.

Boolean statements of look head carry adder

```
p0<= a0 xor b0;

p1<= a1 xor b1;

p2<= a2 xor b2;

p3<= a3 xor b3;

g0<= a0 and b0;
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g1<= a1 and b1;

g2<= a2 and b2;

g3<= (a3 and b3);

c1<= ((p0 and c0) or g0);

c2<= ((p1 and ((p0 and c0) or g0)) or g1);

c3<= ((p2 and ((p1 and ((p0 and c0) or g0)) or g1)) or g2);

Carry (C4) <= ((p3 and p2 and ((p1 and ((p0 and c0) or g0)) or g1)) or g2)) or g3);

s0<= (p0 xor c0);

s1<= (p1 xor c1);

s2<= (p2 xor c2);

s3<= (p3 xor c3);

In structural style of modeling VHDL directly deal with the structure of circuits [8]. Component's ports are mapped to perform the operation of Ripple carry adder. Execution of a model in the software environment is known as simulation. Simulation of both the adders is done by Xilinx ISE Design Suite. The simulation results provide the RTL (resister transfer level) view and output by processing on input. The simulation results of both the adders are given below:

A. Look ahead carry adder

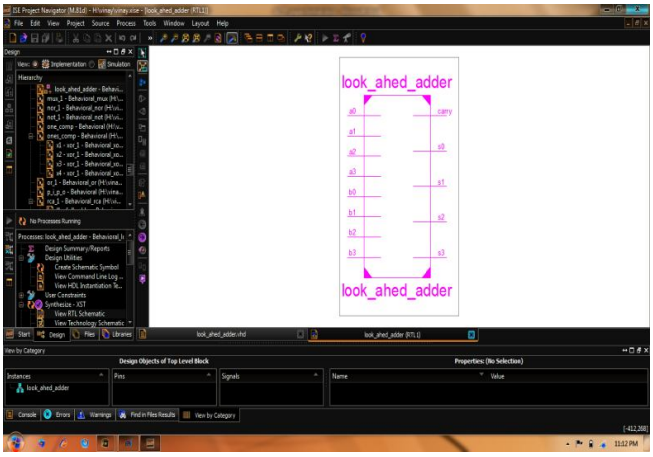

Figure 5 (a): RTL view of LCA

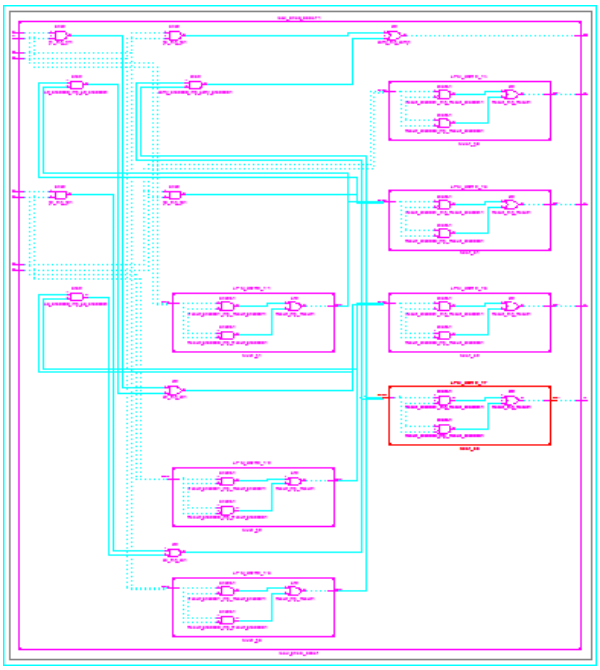

Figure 5 (b): RTL view of LCA

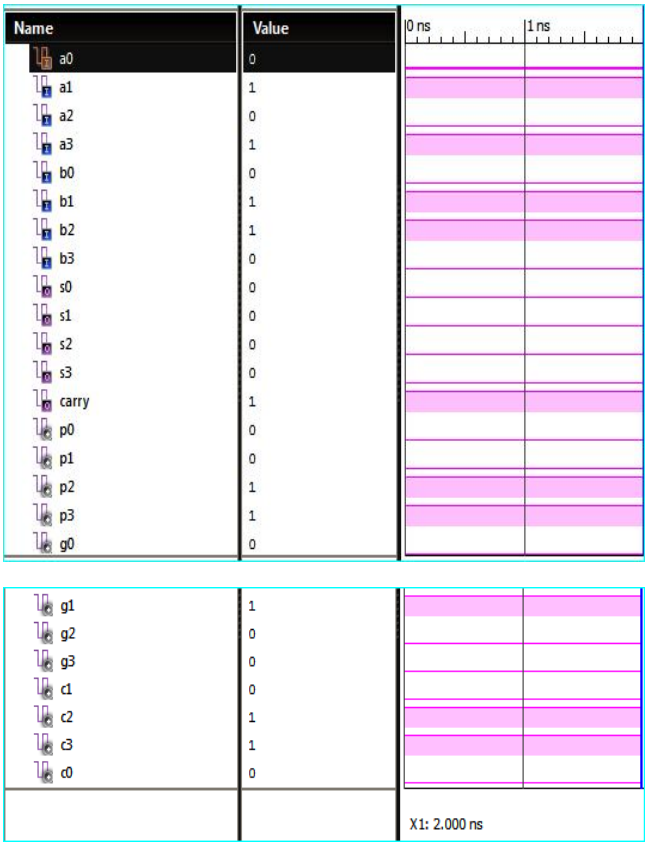

Figure 6: Simulated output waveforms

B. Ripple carry adder

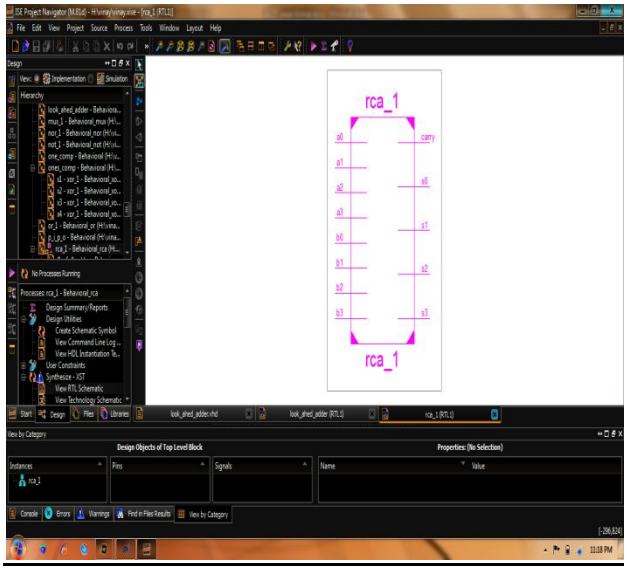

Figure 7 (a): RTL view of RCA

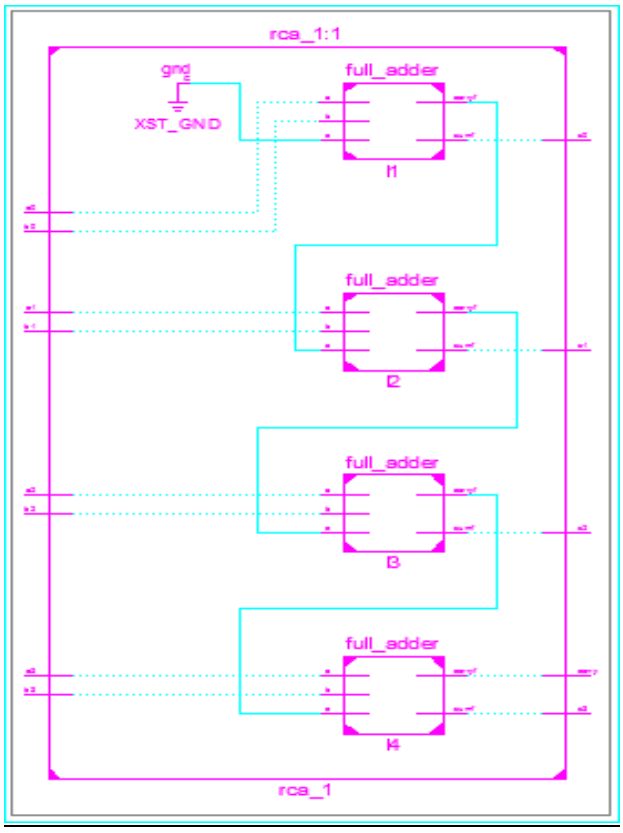

Figure 7 (b): RTL view of RCA

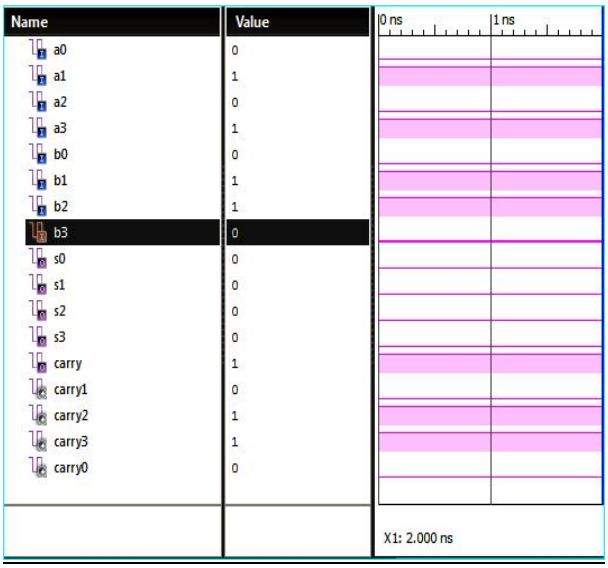

Figure 8: Simulated output waveforms

IV. COMPARISON BETWEEN LCA AND RCA

Performance (speed) is most important parameter of digital circuits. In this paper, look ahead carry adder and ripple carry adder are discussed. In both these adders, look ahead carry adder is fastest than ripple carry adder. Because in LCA, carry is generated by look ahead carry generator in parallel way [5, 6].

In LCA, suppose each gate has a same delay of Tpd. Then to provide carry output LCA is required 3*Tpd delay, and to provide sum output LCA is required 4*Tpd delay. In look ahead carry adder delay is fixed to produce output. Delay does not depend on no. of bits that are being to be added through LCA.

Let each gate delay= Tpd
In LCA delay to provide carry output= 3*Tpd
In LCA delay to provide sum output= 4*Tpd

On the other hand, ripple carry adder's output delay depends upon no. of input bits that are being to be added. Suppose each gate provides Tpd delay. So each full adder will provide (2*Tpd) of delay. To add n-bits RCA will provide (2n *Tpd) delay.

Let each gate delay= Tpd
So, each full adder delay= 2*Tpd
Total delay of RCA to produce n-bits addition= 2*n*Tpd

In parallel adder (RCA) carry is propagated from one stage to other stages. Hence adder will become slow, when no. of bits are increased. To overcome this issue, look ahead carry adder is used [7].

Both of these adders have its importance. Look ahead carry adder is efficient in performance. To speed up, LCA requires more hardware so its cost is more than ripple carry adder. Ripple carry adder is cost effective but poor in performance. So, both of adders are used based upon required situation.

V. CONCLUSION

Design and simulation of Look ahead carry adder and Ripple carry adder has been done. VHDL (very high speed integrated circuit hardware description language) is used to design both of these adders. LCA and RCA both are compared. In results, LCA is fastest adder than RCA but it is not cost effective like Due to carry propagation, RCA is too slow. To overcome this disadvantage of ripple carry adder, look ahead carry adder is preferred.

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