An Improved Low-Voltage Low Power Fully-Differential Double Folded Cascode Class AB Opamp for Pipeline ADC Applications

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***Abstract*—**This paper presents with a fully differential amplifier(FDA) consists high output voltage swing, less susceptibility to common mode noise, and cancellation of even-order nonlinearities of double folded cascode and class AB output with continuous time common mode feedback (CMFB) network ,this function is control the common mode voltage. High-Gain loop consumes less than 1.2mW at 1.8Volts single supply voltage in a 0.18µm CMOS process in Cadence Spectre Circuit Simulator. This circuit design of the CMFB circuit is more challenging than the actual op-amp design due to the difficulty of properly compensating it. However, it is challenging to integrate high-speed, high-resolution ADCs in low cost IC processes, when compared to conventional designs, enabling operation at higher clock frequencies as the class AB stage causes the slew limiting in the first stage and power dissipation is decreasing.

***Keywords*—** *Analog-to-digital converter (ADC); fully differential operational amplifier; common mode feedback (CMFB); class AB; double folded cascode(DFC).*

I. INTRODUCTION

Designing analog-to-digital converters (ADCs) with high bit resolution, low power, low noise ratio and high sampling rate(speed) have five key challenges to be considered. Pipe line ADCs are commonly used for power efficient high speed conversion wide bandwidth input signals and has good accuracy. It offers an attractive combination of speed, resolution, low power consumption and small die size. The speed, accuracy and resolution of pipeline ADC is greater than to flash ADC. It can be implemented in wireless communication systems and can be determined by settling behavior of operational amplifiers, as opamps are integral parts and basic building blocks used in most analog circuits [1]. Settling speed depends on not only a single pole settling, which is the virtual ground and output will settle exponentially with time constant, but also on unity-gain frequency. As System on Chip (SoC) technologies are remarkably increasing, high-performance opamps are used in ADCs significantly. A gain boosted folded cascode architecture is used in the design of amplifier , which is used in the proposed an ADC. Higher speed is required for future application such as wireless communication. ADCs can limit the performance characteristics of wireless devices as they are power demanding blocks, especially in receiver systems to fulfill the required settling-time with minimum current consumption.

An ADCs encapsulates three key performance metrics: speed, accuracy, and power, as well as their associated tradeoffs with respect to the associated technology. Therefore, decreasing the total power dissipation could yield significant power saving. The system is fully differential amplifier to improve accuracy, power supply rejection ratio and minimize the even harmonic distortion are three important advantages that have. In order to obtain higher DC gain, analog designers tend to design multi-stage topologies and these techniques depend on using cascode structures. In other words, keeping a high DC gain, which leads to use multi-stage amplifiers,is done by applying cascode technique. An improved cascode circuit that combines both high gain and high speed is developed. The folded cascode architecture or the mirrored cascode architecture is designed to increase the input and output voltage swings [2]. In order to increase the open-loop gain, cascode techniques are often applied in opamp design. Recently, in low power voltage, class AB output stage is used increasingly when high efficiency is becoming significant in analog designs, and it has high output impedance.

In our designs, a fully differential folded cascode topology is implemented and the gain enhancement is obtained by replacing the regular cascode circuits with active cascode circuits.Our proposed design is based on a fully differential opamp includes a DFC and class AB output stage with continuous time common mode feedback network which is appropriate for driving 12-bit pipeline ADC with foreground calibration. The speed of a pipelined ADC is always limited by the opamp settling time in the S/H "hold" phase. To optimize the speed, need to maximize the loop

transmission bandwidth. The conceptual difference between double and single processing is that, it requires extra feedback to control the output common-mode component in fully differential amplifiers. an operational amplifier in an ADC must be able to drive large output swing in one clock period. For small signals, the settling time of an operational amplifier is mainly dependent on the bandwidth of the amplifier. On the other hand, for large signals, the slew rate of the amplifier becomes a major contributor to the settling time. Therefore, both high slew rate and wide bandwidth are important factors in choosing the right architecture for the amplifier in an ADC. This design provides a much smaller load capacitance to the output of the amplifier that leads higher speed and larger slew rate. An DFC operational-amplifier topology that achieves improved DC gain and common-mode rejection without sacrificing slew rate.

The organization of this paper is as follows: Section II describes existed and the proposed FDAs, Section III reports the simulation results which are achieved in 0.18µm CMOS technology and also comparison with previous works given. Section IV explains tradeoff in speed, accuracy and area. Section V explains pipe line ADCs applications and advantages. The appropriate analysis for testing opamp is explained with suitable opamp application and at last conclusions are drawn in Section VI respectively.

II. FDA DESCRIPTION

An operational amplifier is one of the most important blocks in the design of a pipelined ADC. In this design, a gain-boosted fully differential folded-cascode amplifer is implemented. Based on the gain-boost principle, we are able to boost the DC-gain and achieve a satisfactory settling behavior as well. A fully differential amplifier (FDA) has a wide range of usage because of its innate immunity to common mode signals and clock feed through. It is a DC-coupled high gain folded-cascode opamp is to apply cascode transistors to the input differential pair but using transistors opposite in type from those used in the input stage. The differential-pair transistors Ml and M2 are n-channel transistors whereas the cascode transistors M5 and M6 are p-channel transistors.

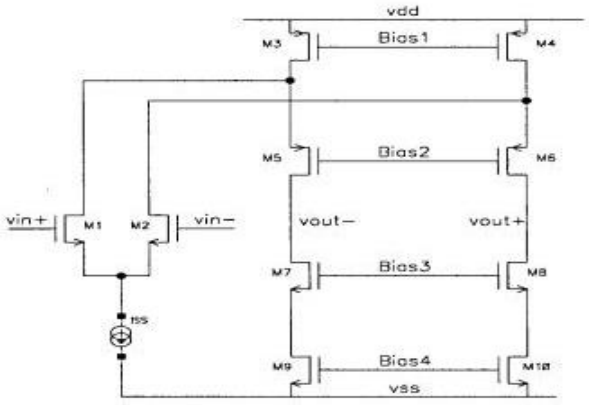

Figure 1. Schematic of fully differential folded cascade opamp

This arrangement of opposite-type transistors allows the output of the amplifier to be taken at the same bias-voltage level as the input signals shown in figure 1., i.e. the output common-mode voltage can be set at the same level as the input common mode voltage, which is convenient for pipelined architecture since the output signal of one stage would be the input for the next stage[3]. FDA is used to convert an analog signal to digital signal and is suitable for driving high-precision ADCs that mostly have differential inputs. Generally CMFB circuits are of two types: Switched Capacitor CMFB circuit and Continuous time CMFB circuit. It has common mode input and differential output[4]. It is needed to stabilize the differential output voltage at a common level. The common mode feed-back (CMFB) is generally needed for two major reasons. Figure 2 shows one is to control the common mode voltages at different nodes that negative differential feedback can stabilize. The other one is to overwhelm the common mode components that tend to saturate with the diversity of stages. Figure 3. shows a general block diagram of a fully differential amplifier with a CMFB.

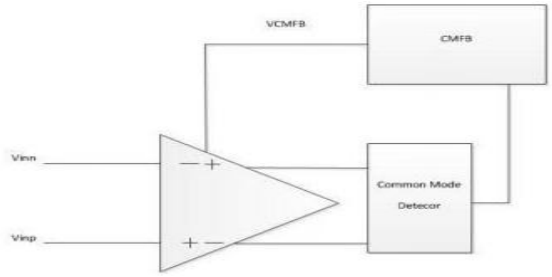

Figure 2 :CMFB

A CMFB circuit has a common mode signal detector and a sense amplifier. Common mode output voltage is the average of the differential outputs. Figure 3 shows a fully differential double folded cascode class AB opamp with continuous time common mode feed-back network (CMFN). Figure 4 shows CMFN is not only a simple element but also it has high common mode rejection ratio (CMRR) which is significantly important in opamp performance, so flowing current must be adjusted carefully.

Generally, to stabilize the common mode voltages for fully differential analog systems in order to adjust common mode currents a CMFN is required. Any increment in bias current is fulfilled by increasing the width of transistors in current source design and this is also valid for composite transistors. If without CMFN, the transistors in system may easily drift away from saturation region due to mismatch and other process tolerances and cause a system malfunction for especially for low voltage applications. In order improve the performance of CMFB, several circuits are proposed, which are resistor averaging circuit, switched capacitor averaging circuit and differential difference amplifier circuits. In this paper presented shown in figure 4. is CMFN circuit for low voltage, large output swing and high speed applications.

Unlike the conventional folded-cascode amplifier, to achieve high slew rate at the output, both PMOS sourcing and NMOS sinking current sources are dynamically controlled with their respective diode-connected transistors. This helps in achieving accurate current sensing. The current sense circuit presented here offers an inherent 180 °phase shift between the class-AB output current and the respective sense currents through current mirrors. Since the current sensing circuit is formed by current mirrors with high quiescent currents, the sensing is fast.

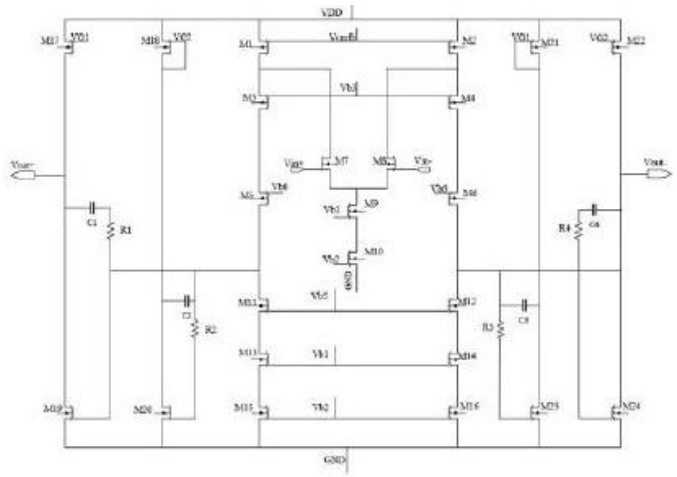

Figure 3. A fully differential double folded cascode class AB

In such a scenario the linear amplifier's power consumption can be reduced by decreasing the bias current such that a minimum required UGF is achieved[5].

Name of Transistor	Length (μM)	Width (μM)	Name of Transistor	Length (μM)	Width (μM)
M1,M2	1	8	M17,M18	0.5	3
M3,M4	0.5	3	M19,M20	0.5	1
M5,M6	0.18	1	M21,M22	0.5	3
M7,M8	0.18	10	M23,M24	0.5	1
M9,M10	1	2	M25,M26,M27 M28,M29,M30	1	8
M11,M12	0.18	0.5	M31,M32 M33,M34	0.28	11
M13,M14	0.5	1	M35	1	2
M15,M16	1	2	M36	1	2

TABLE I .TRANSISTOR SIZES OF PROPOSED OPAMP

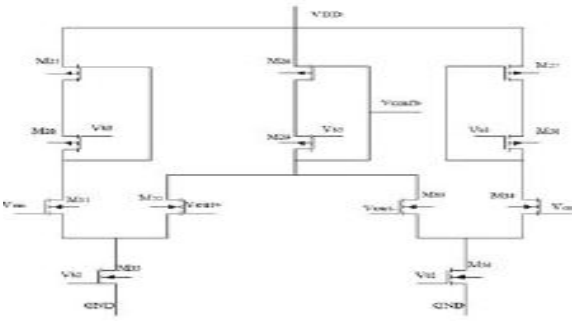

Figure 4 : A fully differential double folded cascode class AB with CMFN.

Significant area savings and a higher cutoff frequency are two main specifications of this design. As it can be observed from Fig. 3, common gate transistors are for increasing gain and to reduce the differential input capacitance.

TABLE II.Design specifications of op-amp and ADC

Specification	Value	units
Power supply,V_{DD}	1.8	Volts
Capacitor,C_L	2	pF
Resistors R_1=R_4	200	Ω
Resistors R_2=R_3	100	
I_{Tail}	160	μA
Capacitors	6	pF
V_{CM}	900	mV
Gain	117	dB
Phase Margin	65	Deg
CMRR	72	dB
Power consumption, P_C	1.2	mW
High Speed	100-300	MS/s
high resolution	10-16	Bits
CMRR	>70	dB
PSRR	>70	dB
Dc gain of common mode path	82	dB
Phase margin of fully differential	82	Deg
Slew rate	12.5	V/— s
Technology	0.18	μm

The minimum size of the capacitors is determined in order to limit the SNR and for the maximum signal swing limited by the power supply.In Table II given design specification of proposed op-amp and pipe line ADCs.

Figure 5. shows the suitable high swing bias network for the proposed opamp. In order to minimize the systematic mismatch error and to scale the circuit with this chosen values.

TABLE III.Representation of Chosen parameters

Chosen Parameters		Values	units
Resistors RP1=RP2		40	kΩŸ
NMOS transistors	Length	1	μM
	Width	2	μM
PMOS transistors	Length	1	μM
	Width	8	μM
Current source		10	μA

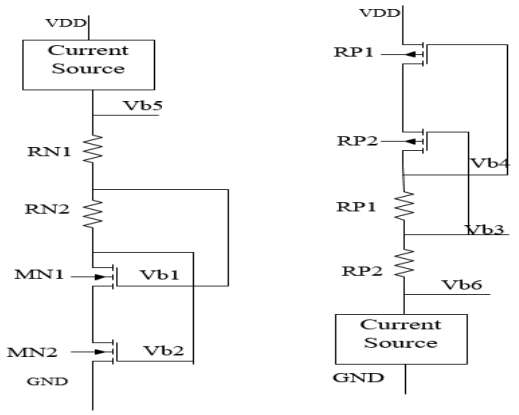

Figure 5 . Biasing circuit of proposed opamp.

III. SIMULATION RESULTS

Fig. 6 shows the qualified setup for doing AC analysis for fully differential and common mode path that gain and phase margin can be obtained. Fig. 7 shows the gain and phase margin of designed opamp which are 117 dB and 65-degree, respectively. Also, Fig. 8 shows the gain of 82 dB and phase margin of 82-degree for common mode path. The transient analysis has been done to V_{O+}, V_{O-}, V_{diff}, and V_{ocom}. Fig. 9 shows transient analysis which illustrates that the settling time

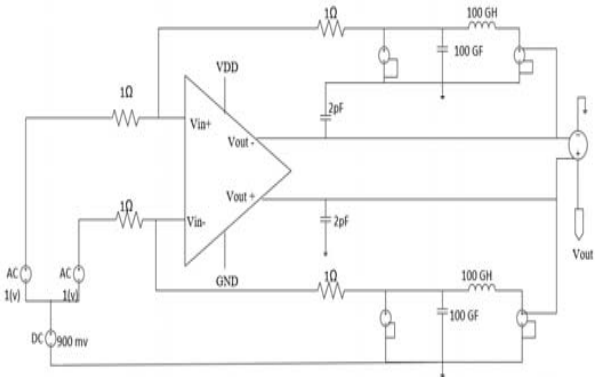

Figure 6. Experimental AC analysis measurement setup for the proposed opamp.

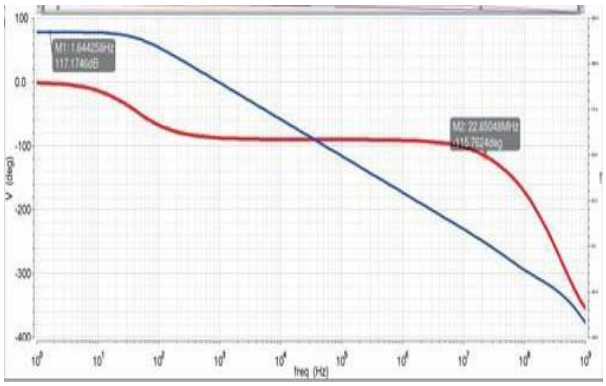

Figure 7. Gain and phase of proposed opamp.

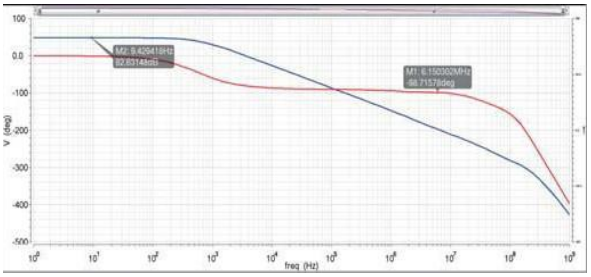

Figure 8. Gain and phase of common mode path.

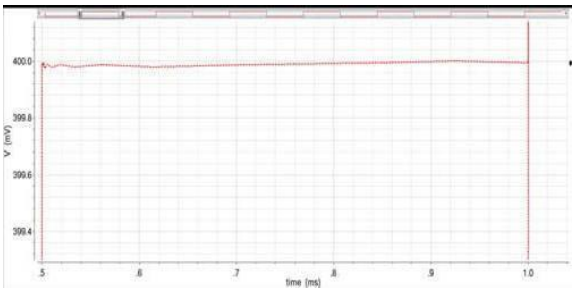

Figure 9. Transient analysis of opamp.

is well enough for driving proposed ADC. In this design, the power consumption is 1.2 mW. The simulation results are given in Table I, and in order to verify the performance of proposed design, comparison with other previous works has been done in Table V which proves it is well suited for ADC applications as it has high gain, high speed, and low power dissipation.

IV. COMPARATIVE DESCRIPTION OF ADCS WITH PROPOSED PIPELINE ADC

Different ADC architectures can be used depending on the required accuracy, speed and power consumption. So there is a tradeoff in speed, accuracy and area. Also it consumes more power.

Comparison of different ADCs

Table IV :Comparison of different ADCs

Architecture	**Latency**	**Speed**	**Accuracy**	**Area**
Flash	No	High	Low	High
SAR	No	Low-Medium	Medium-High	Low
Folding + Interpolating	No	Medium-High	Medium	High
Delta-Sigma	Yes	Low	High	Medium
Pipeline	Yes	Medium-High	Medium-High	Medium
Proposed pipeline ADC	Yes	High	High	Low

In the table, even though the supply voltage and power dissipation in previous works nominated in references 4 to 6 are better than the proposed opamp, their DC gains are

low. Even when considering the work in reference 7, it can be observed that supply voltage and phase margin is better than the proposed opamp, but slew rate is not too appropriate and DC gain is low with respect to our design. Many high performance ADCs are now being designed with differential inputs. A fully differential ADC design offers the advantages of good common-mode rejection, reduction in second-order distortion products, and simplified dc trim algorithms [6]. Although they can be driven single-ended, a fully differential driver usually optimizes overall performance.

Pipelined ADC is a Nyquist –rate analog to digital converter [3]. It is a good choice among other analog to digital converter architectures for sampling rate from few mega samples per second to higher sampling rates. Resolution for such converters ranges from 8 to 16 bits [7]. Pipelined ADC is one of the most efficient ADC used in today's consumer electronics.

TABLE V.COMPARISON OUTCOMES WITH OTHER OPAMPS

Parameters	Proposed	[2]	[5]	Unit
Supply Voltage	1.8	1.2	0.8	V
Power Dissipation	1200	36	1	µW
Slew Rate	12.5	20	0.12	(V/µs
DC Gain	117	33.8	51	dB
Phase Margin	65	45	65	deg

V. PIPE LINE ADC APPLICATIONS AND ADAVANTAGES

Opamps are used as drivers for enhancing the gain and level shifting ,to match the input range of the ADC. The task of selecting appropriate opamp is not straightforward and opamp performance must be measured under identical conditions in ADC applications. Some important specifications are fast settling to ADC transient, high bandwidth, low noise, low distortion, low power, etc. Fig. 7 shows the appropriate 12-bit pipeline ADC with foreground calibration. It is a 12-bit pipeline ADC using three 4-bit stages and one 4-bit flash ADC. In other words, each stage of a pipeline ADC resolves 4 bits and it has a digital error correction logic. Each of the identical stages contains a sub-ADC and MDAC[8]. Calibration parts consist of three 4-bit adders and also three D-Flip flops. Pipeline architecture is appropriate and suitable application for this proposed opamp due to balanced power, speed, and accuracy. Pipelined ADCs are used in a variety of applications such as: mobile systems, CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (e.g. HDTV), Xdsl, cable modems, and fast Ethernet This output result can suffer from errors and the digital data outcome may not represent the real and correct values because of the presence of offset voltages in the comparators of 4-bit flash ADC is shown in Figure 10. Residue transfer curve for a 4 bits/stage is shown in Figure 11 and Figure 12 shows the output of 12-bit pipeline ADC.

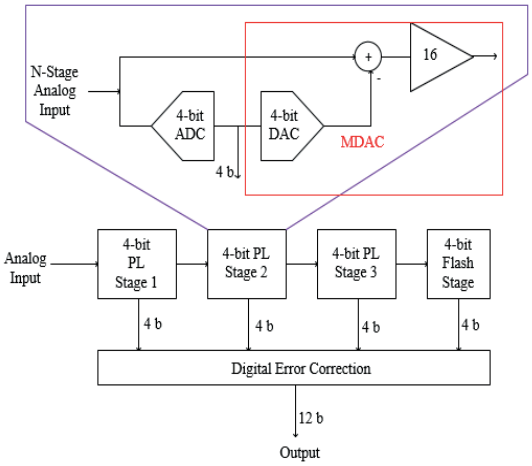

Figure 10. 12-bit pipeline ADC.

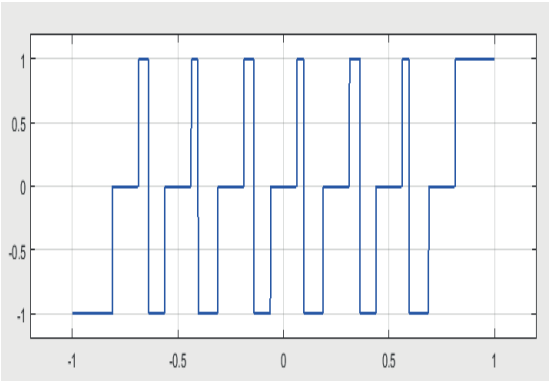

Figure 11. Residue transfer curve for a 4 bits/stage.

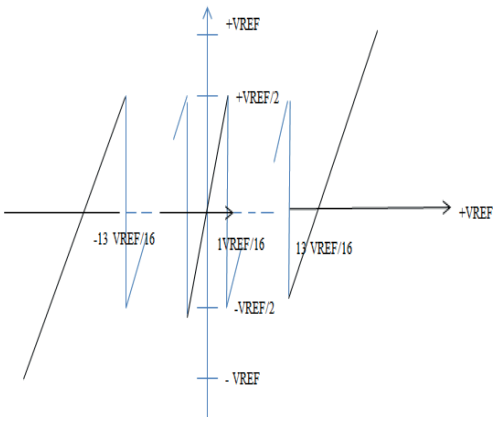

Figure 12. Output of 12-bit pipeline ADC.

Table VI: Pipeline ADC Specifications

Specification	Value	Units
Resolution	12	bits
Sample Rate	200	MHz
Power Supply	1.8	V
Vcm (Op-amp)	900	mV
Power Consumption	1.2	mW
Tail Current	160	µA
Power Supply	1.8	V

VI. CONCLUSION

System design and transistor level design has been done using Cadence Spectre circuit simulator because it provides fast, high precision simulations for mixed-signal circuits and waveforms have been viewed using waveform viewer. In order to define the performance of an ADC, performance parameters play a very vital role and it is really important to ensure that the ADC is working well by measuring its static and dynamic parameters. A fully differential double folded cascode class AB operational amplifier with continuous time common mode feedback network is designed and simulated using cadence simulator in 0.18 µm CMOS process [9]. In order to check and verify the well-performance of the design, different tests have been done and shown good agreement. In Analog-to-Digital converters, high resolution and high speed are two important specifications which our design tries to achieve these where the proposed opamp can be employed as an efficient pipeline ADC driver. The best thing about a pipeline ADC is that it can provide high throughput rates and occupy small die area.

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