Low-Power, High-Performance Optimization of Full Adders in CNFET and FinFET Technology

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Abstract - In this paper, we study the performance of Full Adder circuit with three different FET devices, MOSFET, CNTFET, in 32nm and FinFET in 22nm technology. The full adder circuit is implemented using different logic styles, and compared under the three transistor technology. Average Power consumption and delay of full adder are investigated using HSPICE simulations. Here we find out which one show thebest performance among the three with the least power consumption and propagation delaywhen compared with their counterpart.

Keywords: *Carbon nanotube field-effect transistor (CNFET)32nm, full adder, low-energy, FinFET22nm, MOSFET 32nm.*

I. INTRODUCTION

Addition is the most basic arithmetic operation and usually used in any digital electronic devices and arithmetic logic unit (ALU) to add any value of numbers. The commonly used adder cell is full adder where three inputs i.e. A, B and C_{IN} will be added together to calculate the output of Sum and COUT. The expression for Sum and C_{OUT} is given by:

$$Sum = (\overline{B \oplus C}). A + (B \oplus C) . \overline{A} \quad (1)$$

$$C_{out} = (\overline{B \oplus C}). B + (B \oplus C) . A \quad (2)$$

Where above Equations are generated from the truth table of 1-bit full adder as shown in Table 1. Full adder circuit provides a Sum and a Carry output (Cout) as the result of addition for three input binary digits, named A, B, and Cin. The Cout signal is passed to the higher significant position if it exists. Since a full adder plays a key role in determining the performance parameters of an entire digital system, various designs have been addressed in the literature over years. Each of these designs has its own merits and demerits, in terms of power consumption and speed.

Table 1: Truth table of 1 bit full adder

INPUTS			OUTPUTS	
A	**B**	**C**	**SUM**	**COUT**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

In general, a full adder belongs to either a dynamic or a static style. Although a dynamic style full adder has small on-chip area and high-speed operation compared with a static style full adder, but it suffers from some inherent handicaps, such as susceptibility to leakage, charge sharing, high clock load, and low noise immunity [9]. Therefore,we do not include dynamic full adders in our discussions in this paper. Some recent published static style full adder cells are deeply reviewed in the following. The full adder, based on classical standard complementary metal-oxide semiconductor (CMOS) logic design. This cell is called C-CMOS and consists of 28 transistors. The C-CMOS design does not use complement of input signals, and therefore, the short-circuit current is reduced. Another benefit of C-CMOS is that it produces full voltage swing outputs. The critical path of C-CMOS circuit contains five transistors, which results in long propagation delay. In MOSFET technology, the ratio of size of pMOS to nMOS should be almost three to have equal switching speed between them and good noise margin for the circuit. This causes the existence of large input capacitance in MOSFET technology and consequently more delay and power dissipation. On the other hand, since in CNFET technology, the both p-type (pCNFET) and n-type (nCNFET) transistors have equal current driving capability with the same transistor dimension [18], their sizes are set, such that to be equal. In conclusion, in the CNFET technology, the input capacitance of C-CMOS cell will be small. Another complementary design, namely Mirror, is reached with a cleverly change in the structure of C-CMOS. The Mirror uses the same number of transistors as used in the C-CMOS and consumes almost equal power dissipation. The main difference is that the maximum propagation path of the Mirror consists of four transistors, which is smaller than that of the C-CMOS. Therefore, the Mirror design is expected to be faster than the C-CMOS design. The TFA circuit is based on transmission function theory. The maximum propagation path of the TFA contains four transistors. The TFA is constructed using 16 transistors. The power consumption of the TFA is expectedto be lower than that of the C-CMOS and Mirrorcells due to lower transistor countand lower input capacitances.It is worth to point out that the TFA has not driving outputs, and its performance will significantly degrade either in the presence of large fan-outs or in a cascaded configuration. This is due to coupling the inputs to the outputs of the circuit. The design of a transmission gate full adder (TGA)The TGA comprises 20 transistors, and its critical path has four transistors. The same as the TFA, since the inputs of the

TGA cell are coupled to the outputs, it suffers from lacking driving power. Lacking driving capability drastically degrades the performance of the TGA, where it is employed in a cascaded structure or where there are large fan-outs. One solution to alleviate the performance degradation is to put buffers at the output nodes between consecutive cascaded stages. However, this approach results in transistor count overhead and removes the
advantage of small transistor counts in large cascaded circuits. The TGA cell performs better than the TFA due to employing TGs at the output nodes instead of pass transistors. In fact, its delay and power dissipation are less than that of TFA, especially in larger circuits. The CPL-TG not only is dual rail but also provides driving capability at the expense of large transistor count. Then, it is advantageous in the cascaded circuits. To generate the XOR/XNOR functions, it uses CPL.

II. PROPOSED METHODOLOGY & SIMULATION RESULTS

Proposed Full Adders shows six different designs of full adder cells, which employ hybrid logic style. Show below Fig.1 to fig.6 is produced by replacing the XOR/XNOR module with the proposed XOR/XNOR cells shown in fig. below. All these full adder cells provide delay and average power capability by decoupling inputs and outputs. Furthermore, the full adder without driving outputs that we intentionally include in our simulations to show the effect of output driving power in determining performance measures of full adders. This design is realized by replacing the XOR/XNOR module presented with the XOR/XNOR circuit .We are later intended to clarify the advantage of full adders over the block diagram shown in Fig.1 the schematic of the first proposed full adder cell, which employs PTL to provide XOR/XNOR functions.

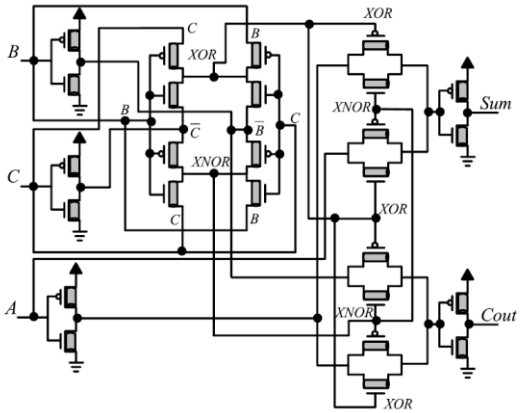

Figure 1: Pass-Transistor Full Adder (FA-Design 1)

The pass-transistor full adder (PT-FA) consists of 26 transistors. The critical path of the PT-FA consists of four transistors. This structure provides a good driving capability, using NOT gates at the output nodes. In fact, it guarantees the proper functionality when it is embedded inside large circuits in a cascaded form. Nonfull-swing outputs of XOR/XNOR circuits embedded in the PT-FA cause leakage current and consequently large power consumption. Feedback loop transistors in the XOR/XNOR circuit of the Feedback Loop-Full Adder (FL-FA) full adder,shown in Fig. 2, restore the non-full-swing outputs of the XOR/XNOR circuit. The FL-FA contains more transistors compared with the PT-FA, 28 transistors.

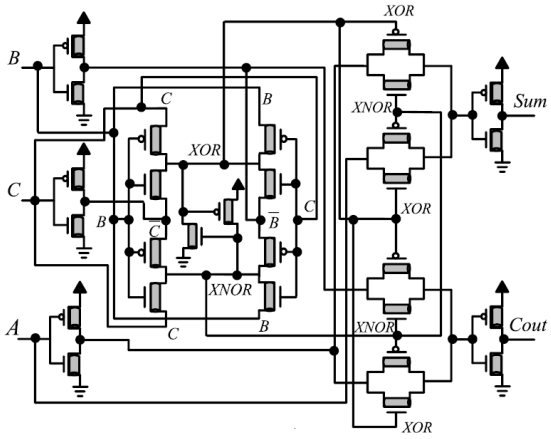

Figure 2: Feedback Loop-Full Adder (FA-Design 2)

The critical path of the FL-FA consists of four transistors. The same as the PT-FA, inverters at the output nodes of FL-FA provide desired driving power for the following cells. Feedback loop transistors decrease power consumption by generating full output voltage swing and removing static power dissipation, while feedback loop decreases the delay of circuit as well. The other proposed full adder, which contains double driving path for XOR/XNOR circuits, called Double Driving-Full Adder (DD-FA), is shown in Fig.3. The DD-FA employs transmission function along with PTL logic to produce full-swing outputs for the XOR/XNOR circuit.

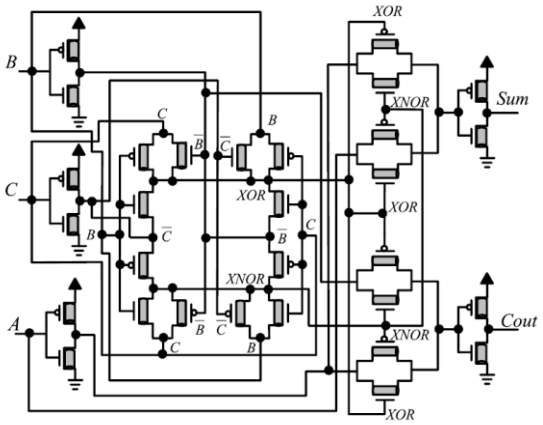

Figure 3: Double Driving-Full Adder (FA-Design 3)

It contains 30 transistors, and the propagation delay consists of four transistors. Since TG is inherently a low-power circuit, the power consumption of the DD-FA is less than the PT-FA and FL-FA circuits. The fourth proposed full adder shown in Fig.4 that contains single driving path for

the XOR/XNOR circuit is called -Single Driving-Full Adder (SD-FA), and has 28 transistors.

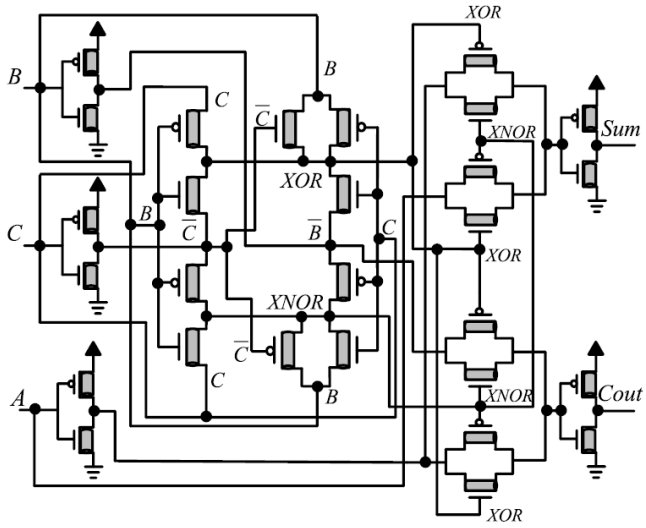

Figure 4: Single Driving-Full Adder (FA-Design 4)

It uses TG and PTL logics to produce desired outputs, the same as the DD-FA. The difference between DD-FA and SD-FA is that the SD-FA cell employs only two TGs to generate full voltage swing intermediate outputs (i.e., the outputs of the XOR/XNOR circuit). Thus, it has two fewer transistors than the DDFA and consumes slightly lower power. The design shown in Fig.5, which removes two pass transistors of single driving path of the XOR/XNOR circuit, is called -Removed Single Driving-Full Adder (RSD-FA). This design removes two pass transistors while at the same time maintaining the rail-to-rail outputs for the XOR/XNOR circuits.

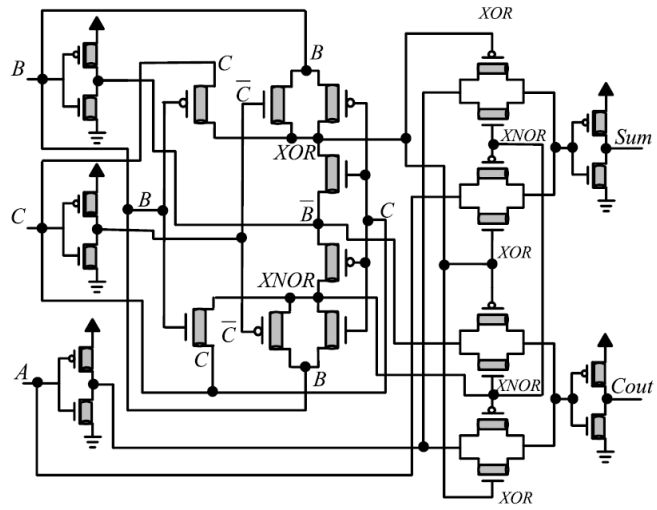

Figure 5: Removed Single Driving-Full Adder (FA-Design 5)

The same as the other proposed full adders, it benefits driving capability. The RSD-FA has 26 transistors, which is less than the transistors of FLFA, DD-FA, and SD-FA. Therefore, it is expected to have the least power dissipation compared with others. Fig.6 a full adder cell with non-driving power called Non Driving-Full Adder (ND-FA). The ND-FA produces full-swing outputs because of applying TGs in its structure.

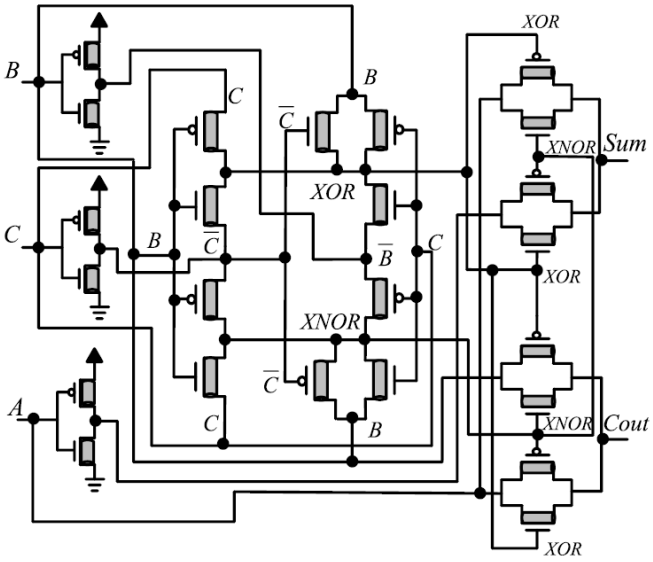

Figure 6: Non Driving-Full Adder (FA-Design 6)

Unlike the previous ones, the ND-FA suffers from lacking driving power due to coupling inputs to outputs. On the other hand, a remarkable advantage of the ND-FA is that it is faster than the previous proposed full adders because of three transistors being in its critical path. The minimum transistor count, which is 24 transistors, belongs to the ND-FA design. Note that the ND-FA performs well when used solely in the presence of small fan-outs; but when it is used in the presence of larger fan-outs or cascaded structures, its performanceis decreaseddramatically.

III. SIMULATION RESULTS

The Adder Circuits is simulated on HSPICE Software tool. The model used for FinFET circuit analysis is BSIM-CMG for 32nm FinFET device. BSIM-CMG is a model for MG transistors which are implemented in Verilog-A and models for 32nm MOSFET and 32nm CNTFET from PTM website. This model describes all the important behaviour of MG transistor. It is physics based model which is scalable and predictive over a wide range of device parameters [12].

In table 2, Average power consumption, delay and PDP are shown, it is seen that FinFET based Full adder design show best performance on the basis of Power, Delay and PDP.

Table 2: Average Power Consumption, Delay and PDP Comparison.

AVERAGE POWER CONSUMPTION (E-6 W), DELAY (E-11 S), PDP (E-17 J)

Name	MOS			CNFET			FinFET		
	Power	Delay	PDP	Power	Delay	PDP	Power	Delay	PDP
FA-Design 1	17.400	71.500	1244.100	0.290	6.430	1.865	0.046	6.440	0.294
FA-Design2	34.900	68.000	2373.200	0.317	3.500	1.110	0.081	6.730	0.546
FA-Design3	38.400	72.600	2787.840	0.189	7.580	1.433	0.084	16.000	1.336
FA-Design4	31.200	70.100	2187.120	0.194	3.490	0.677	0.088	13.200	1.159
FA-Design5	23.200	72.600	1684.320	0.204	3.330	0.679	0.083	15.400	1.281
FA-Design6	29.600	17.300	512.080	0.155	0.052	0.008	0.079	0.064	0.005

In table 3, Average power consumption, delay and PDP with variations in Vdd, 0.9v, 1.0v and 1.1vare shown, it is seen that FinFET based Full adder design show best performance on the basis of Power, Delay and PDP. With variation of power supply, it is seen that with 0.9v Vdd, Average power is reduced but delay is increased, best optimization can be achieved at vdd=1v.

Table 3: Average Power Consumption, Delay and PDP Comparison (Vdd Variations)
AVERAGE POWER CONSUMPTION (E-6 W), DELAY (E-11 S), AND PDP (E-17 J) RESULTS FOR DIFFERENT POWER SUPPLIES

Name		CNFET			FinFET		
		Power	Delay	PDP	Power	Delay	PDP
Vdd =0.9V	**FA-Design 1**	0.150	12.700	1.905	0.018	12.800	0.230
	FA-Design2	0.190	13.500	2.565	0.038	9.690	0.371
	FA-Design3	0.104	13.100	1.362	0.028	43.800	1.231
	FA-Design4	0.104	11.700	1.217	0.031	20.600	0.634
	FA-Design5	0.107	12.000	1.284	0.036	20.700	0.741
	FA-Design6	0.068	0.021	0.001	0.024	0.102	0.002
Vdd =1.0V	**FA-Design 1**	29.000	6.430	186.470	0.046	6.440	0.294
	FA-Design2	31.700	3.500	110.950	0.081	6.730	0.546
	FA-Design3	18.900	7.580	143.262	0.084	16.000	1.336
	FA-Design4	19.400	3.490	67.706	0.088	13.200	1.160
	FA-Design5	10.400	3.330	34.632	0.083	15.400	1.281
	FA-Design6	15.500	0.051	0.794	0.079	0.064	0.005
Vdd =1.1V	**FA-Design 1**	0.434	6.410	2.782	0.078	5.870	0.457
	FA-Design2	0.621	6.240	3.875	0.116	5.470	0.635
	FA-Design3	0.365	6.360	2.321	0.155	4.340	0.673
	FA-Design4	0.391	7.480	2.925	0.138	4.120	0.569
	FA-Design5	0.405	6.430	2.604	0.160	4.140	0.662
	FA-Design6	0.303	0.089	0.027	0.115	0.058	0.007

In figure 7, Average Power consumption of FinFET and CNFET based full adders. It is clear that FinFET based have best average power consumption, especially for circuit full adder design 1.

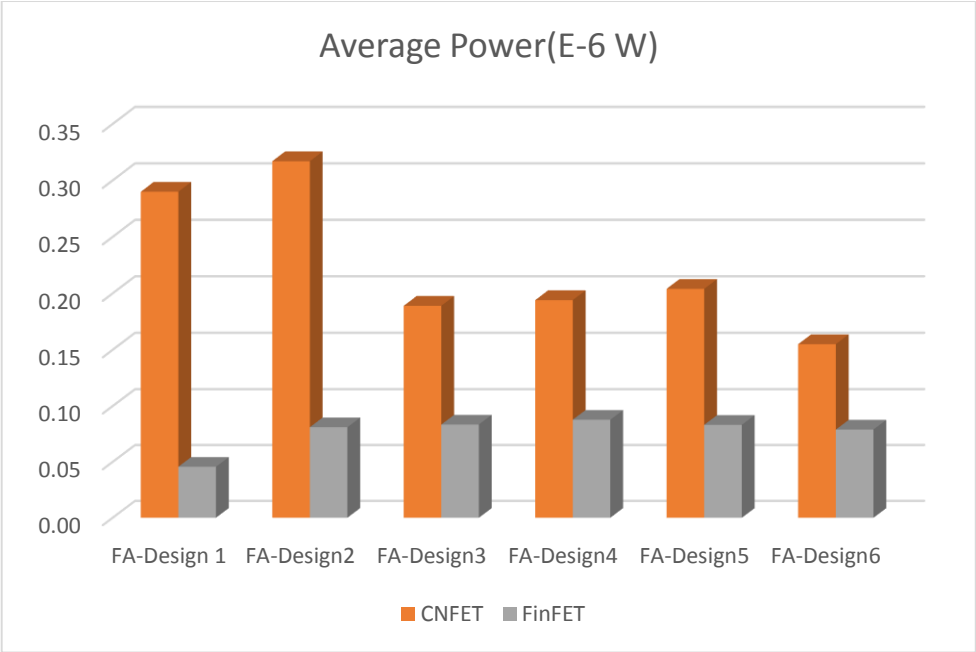

Figure 7: Average Power Consumption for MOS, FinFET and CNFET for all Full Adder Design

In figure 8, Delay of FinFET and CNFET based full adders. It is clear that FinFET based have best delay in Full adder design 6. In Full Adder design 4 and 5, Delay is increased in FinFET based circuits.

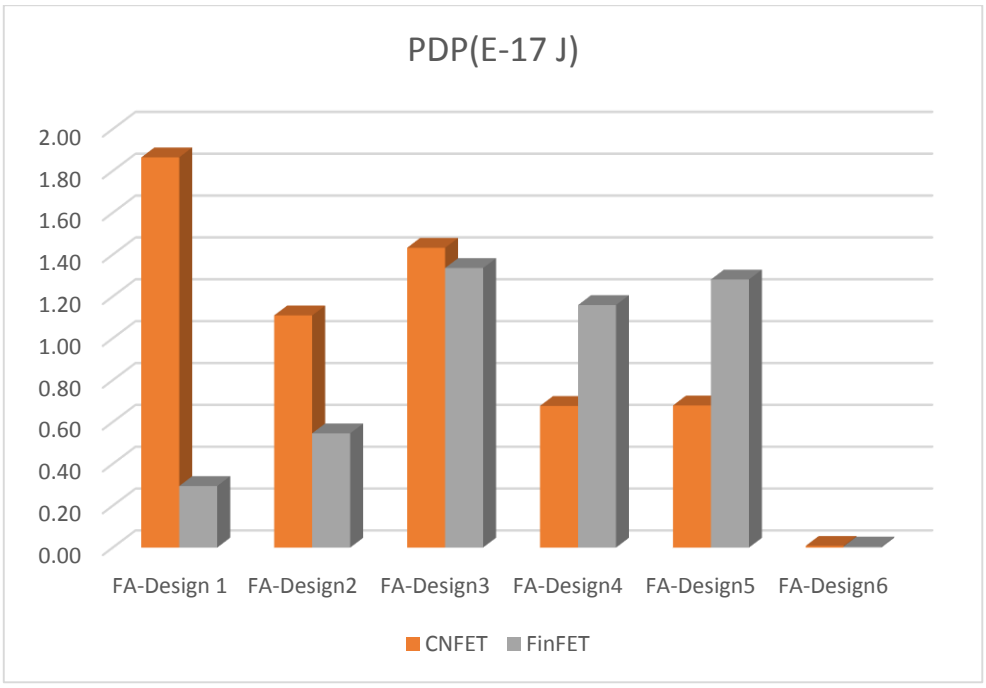

Figure 8: Delay for MOS, FinFET and CNFET for all Full Adder Design

In figure 9, PDP with variation of NFIN that is number of fins is shown in FinFET based Full adders. Minimum PDP is seen in Full Adder design 6.

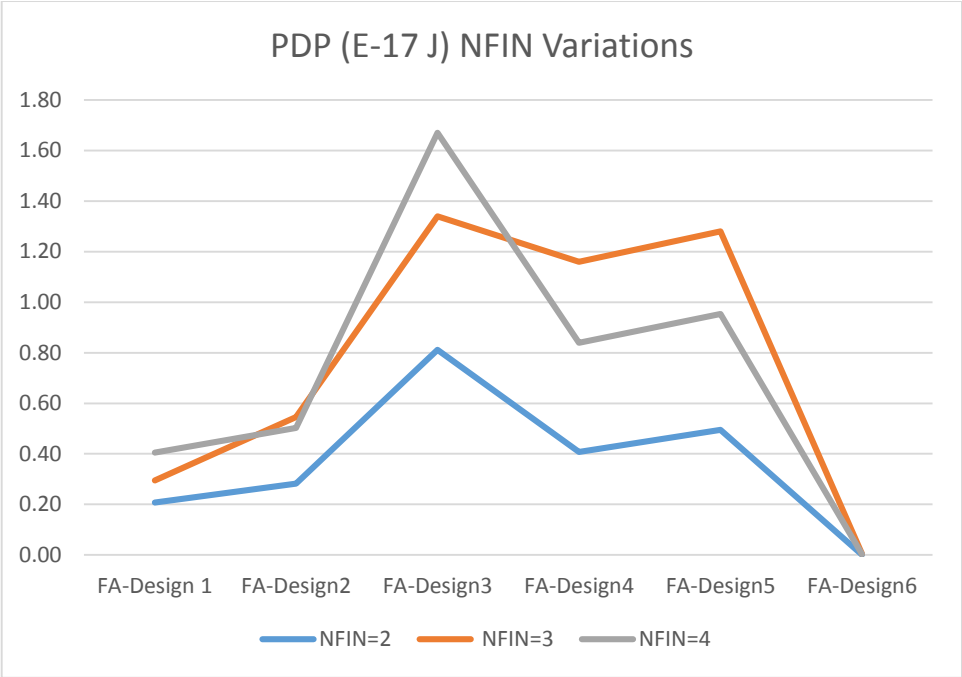

Figure 9: PDP NFIN Variation

IV. CONCLUSION

In this paper, a high-speed and high-performance FinFET-based Full Adder cell for low-voltage applications has been proposed. The Sum and Cout generator modules of this Full Adder, which are fully symmetric and have the same hardware configurations, produce the Sum and Cout signals in a parallel manner. The great advantage of the proposed cell is its very short critical path, which consists of only two CNFETs. This leads to very short propagation delay and also makes this design appropriate for lowvoltage applications. Results of the comprehensive simulations demonstrate considerable improvements in terms of delay and in terms of average power in comparison with the other conventional and technology 32-nm MOSFET and CNFET-based Full Adder cells, in various situations. Full Adder design 6 is improved by the use of FinFET technology on basis of Average Power Consumption, delay and PDP. Power is improved by 84.13% when compared to CNTFET, 37.5% improved is seen in PDP for FinFET based FA Design 6.

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