

Research Article

Design of Multistage Amplifier for Small Signal Audio Applications

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Abstract

The proposed multistage amplifier can be used in audio applications. It is designed by using cascade connection with BJT and FET. The multistage amplifier has only one input that is ac signal (sin wave) and output is audio signal. The amplifier is working at a resonance frequency of 1 KHz to 3 MHz and it is designed by using pspice software. The proposed amplifier hardware setup is done by breadboard. The gain of the multistage amplifier is very low and the frequency is maintaining constant at particular level (31.16 gain).

Keywords: Field effect transistor; Bipolar junction transistor; Common source circuit; Common emitter circuit.

Introduction

Common emitter

The basic common emitter circuit is connected with voltage divider biasing. The emitter is common for both base and collector. So, the emitter is in the state of ground potential. Hence it is named as a common emitter. Its frequency range is high. In this, coupling capacitor act as a perfect short circuit. The input signal voltage and input base current are given in the form of phase, such frequency is in the midrange frequency. We need to apply equivalent circuit of the bipolar junction transistor that was previously developed. In general, the hybrid-II model is used throughout the text [1-2].

Common source

The basic common source circuit is connected with voltage divider biasing. We are able to see that the source is common for both drain and gate. Hence, it is named as a common source. The signal that comes from the signal source is coupled into a gate of the transistor through the coupling capacitor. The frequency range of the signal is very high. The small equivalent circuit with coupling capacitors are connected in short circuit. In common source circuit, minimum input and voltage is produced. And the output impedance leaves the current [3-4].

Multistage amplifier

The transistor amplifier circuits can be connected in cascaded. There are two transistors used, one transistor is Field Effect Transistor (FET) and another transistor is a Bipolar Junction Transistor (BJT). The small signal equivalent circuit all the capacitor act as a short circuit. The amplification should be done at a suitable location along the transmission link to boost up the signal level. In audio amplifier the frequency range is 20 Hz to 20 KHz [5]. The power gain of the amplifier is the ratio of the output power to the input power. The overall gain is obtained by multiplying the gain of the individual stage, when we have passive coupling network between amplifier stage. The absolute power level of the output in the amplifier is sometimes specified in dB [6]. A practical signal is usually complex (contain many frequencies). That is due to the various frequency depends only on reactance (capacitance and inductance) present in the circuit [7-8]. The active devices are BJT and FET. The frequency response of an amplifier is plotted between the gain and frequency. If the gain is constant in the particular frequency (1 to 10 KHz), the frequency response of an amplifier is divided into three regions. (i) The mid band frequency region, over which the gain is constant. (ii) The lower frequency region, Here the amplifier behaves like a high pass filter. (iii) The higher frequency region, in this the

circuit, it behaves like a low pass filter. Hence there is a voltage drop across the resistance (Rs). The voltage gain of the amplifier decreases at high frequencies. When the cascade stage is given in a large output, the overall gain is equal to the product of the individual stage gain [8-10].

Design of multistage amplifier

First, we replace the transistors in the circuit BJT and FET with the model of small signal equivalent circuit, and we have to write equations for DC bias, then we restore the transistors in the circuit voltage equation which are solved, the voltage gain (Av), Input resistor (Rin), Output resistor (Ro).

D.C. Bias equations

The equations Av, Rin, and Rout, along with the D.C. biasing equations are specified. The DC bias equations are formed by writing KVL around the base and collector loops of each transistor giving, where V_b and R_b are obtained by Thevenin equivalent circuit. The bias network in the usual way.

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Common emitter

The collector current is found out by the product of gain and base current,

$$I_C = \beta I_B = 2mA$$

The emitter voltage is can be obtained by multiplying the corresponding the current and resistance in the emitter terminal,

$$V_E = I_E R_E = 2.42V$$

Writing a KVL equation around a collector terminal, assuming the transistor is bias in the forward active mode, we have

$$V_{CC} = I_C R_C + V_C = 15V$$

The voltage at the base terminal can be found by the difference between base emitter voltage and emitter voltage,

$$V_B = V_{BE} - V_E = 3.1V$$

The base emitter voltage is defined as the difference of base voltage and emitter voltage,

$$V_{BE} = V_B - V_E = 0.7V$$

By using voltage divider circuit, the Thevenin's equivalent resistor value R_1 is,

$$R_1 = \frac{V_{CC} \cdot R_2}{V} - R_2 = 44.0K\Omega$$

Common source

The source voltage is given by the product of current and resistance in the source terminal,

$$V_S = I_S R_S = 1V$$

The voltage at the gate source is given by the difference between gate voltage and source voltage,

$$V_{GS} = V_G - V_S = 2.4V$$

The gate voltage is the difference of gate source voltage and source voltage,

$$V_G = V_{GS} - V_S = 3.4V$$

Results and discussion

To examine the effect of proposed circuit, we fabricated a distributed amplifier using cascade connected BJT and FET terminal circuit. The BJT and FET performs the high-performance super self-aligned process. Results experimental verification for both hardware and software are shown in Fig. 1 and 2.

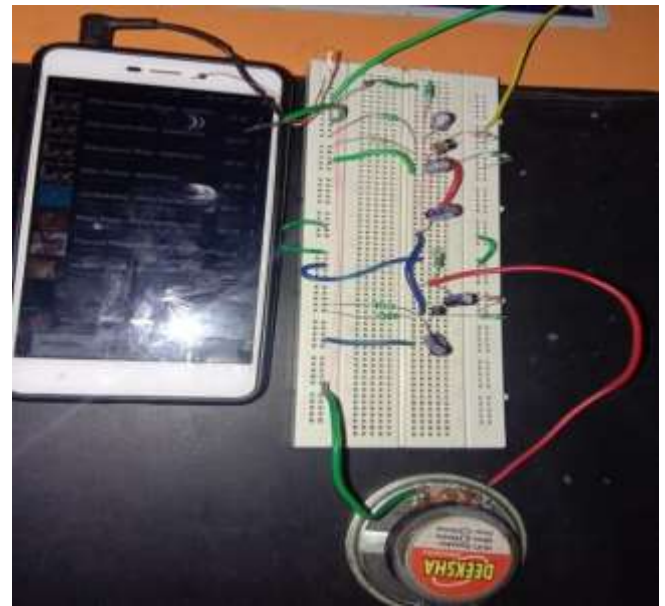


Fig. 1. Experimental results of multistage amplifier

For the gain of the frequency is increases and the frequency is maintained at constant particular level of 31.16 and the frequency gain suddenly decreases. Thus, the software and the hardware models expel the output for the multistage amplifier in the range of low gain. It is used to reduce distortion. Hence, they are used

for many applications using the multistage amplifier. The multistage amplifier is designed

on the cascade connected circuit. They have wider bandwidth which was three.

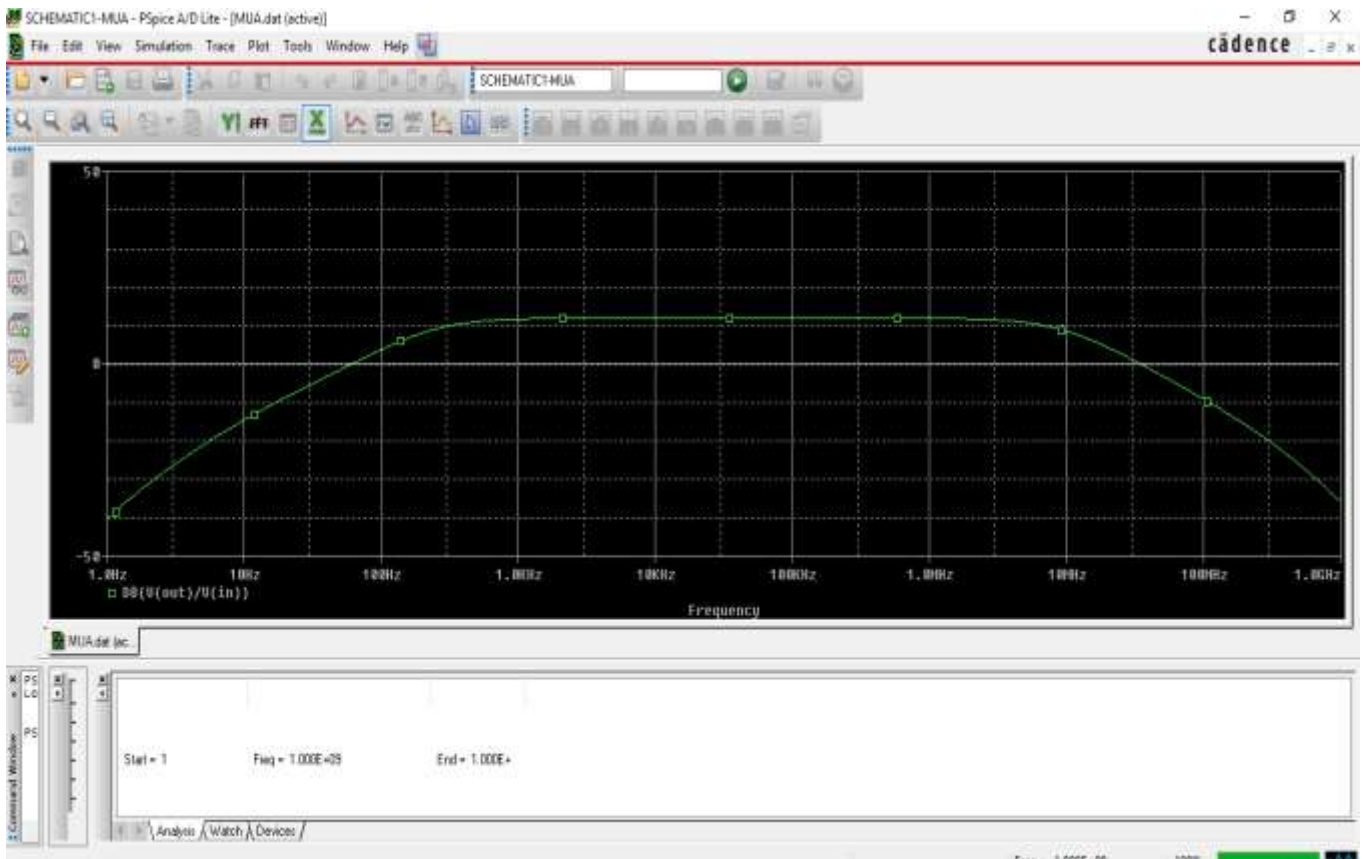


Fig. 2. Simulation results of multistage amplifier

From experimental results we can analyze the multistage amplifier is used for small signal applications. The normal working frequency range is 20 Hz - 200 KHz but the proposed amplifier working under the frequency range is 1 KHz-600 KHz. Here two transistor connected in cascade connection with one capacitor. BJT transistor working under common emitter configuration and FET transistor working under the common source amplifier. The two configurations only the transistor working at maximum gain.

Conclusions

Hence, the simulated multistage amplifier shows better gain and good impedance. The proposed amplifier designed using pspice and hardware setup done by breadboard. The amplifier is satisfied for small signal audio applications. It includes gain, bandwidth and frequency it's capable of produce small audio signal. The simulation output matched with the experimental output.

Conflicts of Interest

Authors declare no conflict of interest

References

- [1] Barataud D, Campovecchio M, Nebus JM. Optimum design of very high-efficiency microwave power amplifiers based on time-domain harmonic load-pull measurements. *IEEE Trans Microw Theory* 2001;49:1107-12.
- [2] Yuan H, Jeong HM, Lee JS, Kang BH, Yeom H, Lee SW, Kim SH, Shin JK, Kang SW. Benzene gas detection using a MOSFET-BJT hybrid mode operated gated lateral BJT. *International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*. 2013: pp. 254-57.
- [3] Kyung-Suk S, In-Young C, Young JP. A BJT-Based Hetero structure 1T-DRAM for Low-Voltage Operation. *IEEE Electron Device Letters* 2012;33:14-6.
- [4] Dong-Il, Sung-Jin C, Jin-Woo H, Sungho K, Yang-Kyu C. Fin-Width Dependence of BJT Based 1T-DRAM Implemented on Fin FET. *IEEE Electron Device Letters* 2010;31:909-11.

- [5] Zhenming Z, Jerry GF, Zhichao L. Physical Insights on BJT-Based 1T DRAM Cells. *IEEE Electron Device Letters* 2009;30:565-7.
- [6] Amin AR, Salehi A; Gheze layagh MH. BJT circuits simulation including self-heating effect using FDTD method. *Asia-Pacific International Symposium on Electromagnetic Compatibility*. Beijing, China. 2010: pp. 924-7.
- [7] Shiwei L, Jun W, Zhigao P, Guanghui C, Xin Y, John Shen Z, Linfeng D. A modified behavior spice model for SiC BJT, *IEEE Applied Power Electronics Conference and Exposition (APEC)*. San Antonio, TX, USA. 2018: pp.238-43.
- [8] Marc A, Nadine C, Robin D, Zhichao L, Bart DW. BJT-Mode Endurance on a 1T-RAM Bulk FinFET Device. *IEEE Electron Device Letters* 2010;31:1380-2.
- [9] Shiwei L, Linfeng D, Zhigao P, Yize S, John Shen Z, Jun W. A New Proportional Base Driver Technique for Minimizing Driver Loss of SiC BJT. *IEEE Energy Conversion Congress and Exposition (ECCE)*. 2018: PP. 5485-8.
- [10] Dapeng S, Man-Kay L, Bo W, Pui-In M, Rui PM. Piecewise BJT process spread compensation exploiting base recombination current. *IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, MD, USA. 2017. pp. 1-4.
