High Speed and Energy Saving Carry Skip Adder

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***Abstract*—**VLSI technology is to optimize any type of digital architecture because this optimization is mainly used to enhance the various applications. A high speed and low energy carry skip adder (CSKA) structure has been proposed here. The speed enhancement is realized by applying concatenation and incrementation schemes to increase the efficiency of the conventional CSKA structure. Rather than utilizing the multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure increases the speed and energy factors of the adder. A hybrid variable structure reduces the power consumption without influencing the speed, is done. The proposed structures are estimated by comparing their speed, power, and area parameters with those of other adders in Xilinx ISE using VHDL.

***Keywords*—**Carry skip adder (CSKA), high performance, energy efficient, AOI/OAI, hybrid variable latency adder

I. INTRODUCTION

Low power adder circuits have become very vital in the VLSI industry due to the quick growth of laptops, portable personal communication systems. Adder circuit is one of the main building blocks in any DSP processor. An adder is the main component in any arithmetic unit. Addition is a basic operation of any digital system, DSP or control system. The fast operation of a digital system has great influence based on the performance of the resident adders. Adders play important component in digital systems because widely used in other basic digital tasks such as subtraction, multiplication and division etc. The increasing performance of the digital adder increases the execution of different binary operations in a circuit consisting of different blocks. The emergence of the digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed.

There are many adders such as ripple carry adder (RCA), carry increment adder (CIA), conventional carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs). In previous method, we are using multiplexer logic in which the number of gate count required is more. Figure 1 shows the conventional structure of carry skip adder. The power consumed by the carry skip adder with multiplexer logic is more and critical path delay is high.

The ripple carry adder is formed by cascading number of full adders (FA) blocks in the series. One complete full adder is responsible for the addition of two binary digits at different stage of the ripple carry. The carry output of one stage is fed directly to the carry-in on the next stage. A number of full adder outputs are added to the ripple carry adder circuit or ripple carry adders of different sizes may be cascaded in order to accommodate the binary vector strings of larger sizes of adders.

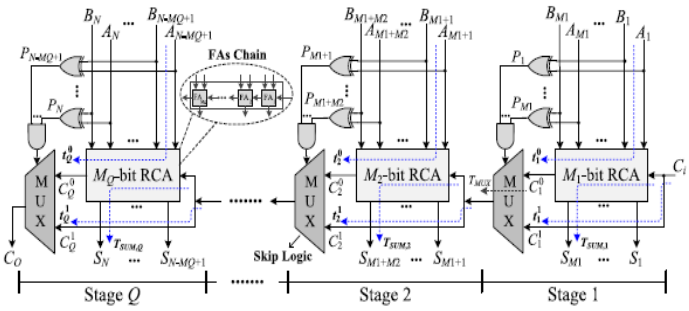

Fig. 1. Conventional structure of the CSKA

For an n-bit parallel adder, it requires n computational elements (FA). The carry is propagated in a serial computation [1]. Delay is high as the number of bits is increased in RCA.

The rest of this paper is organized as follows. Section II discusses related work on the proposed CSKA structure for improving the speed and for increasing the efficiency of adders. In Section III, Proposed hybrid variable CSKA is explained, while Section IV describes the results and discussion. Finally, the conclusion is given in section V.

II. PROPOSED WORK

The focus is on the speed of the carry skip adder structure and the reduction in the critical path delay. The proposed system consists of the ripple carry adder structure with the AOI and OAI compound gates for skip logic. The skip logic reduces the number of gate count in the structure [2]. The speed of the structure is achieved by using skip logic, and the delay is reduced. The conventional structure of the CSKA consists of stages containing a chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). The RCA blocks are attached to each other through 2:1 multiplexers, which can be used in one or more level structures [9]. The CSKA configuration (i.e., the number of the FAs per stage) has a great influence on the speed of this type of adder.

Figure 2 shows the adder contains two N bits inputs, A and B, and Q stages. Each stage comprises of an RCA block with the size of Mj (j = 1,...,Q). The carry input of all the RCA blocks, but for the first block is C_i, is zero (concatenation of the RCA blocks). All the blocks of the structure and execute their jobs simultaneously.

All the RCA blocks, except for the 1st block having zero as carry input. Output carries of the RCA blocks are calculated in parallel.

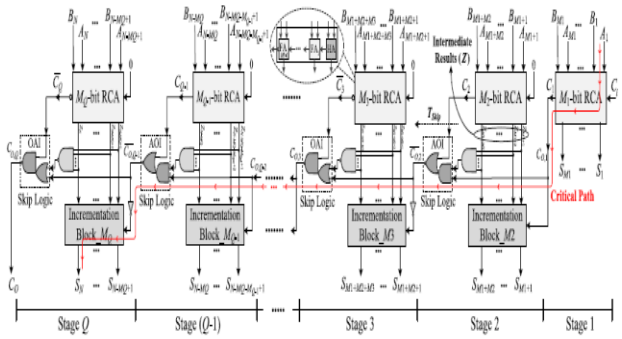

Fig. 2. Proposed CI-CSKA structure.

A. Ripple Carry Adder

The ripple carry adder structure is constructed by cascading full adders (FA) blocks in the series. One full adder is dependable for the adding of the two binary digits at different stage of the ripple carry [8]. The carry out of one stage is fed directly to the carry-input to the next stage. A number of full adder circuits may be added to the ripple carry adder. For an n-bit parallel adder, it requires n number of computational elements (FA). The worst-case delay of the RCA is when a carry signal propagates ripples through all the stages of adder chain from the LSB to the MSB, which is approximated by:

$$T = (n-1)\,tc + ts \quad (1)$$

where the tc is the delay through the carry stage of a different full adder, and ts is the delay used to compute the sum of the last stage.

B. Skip Logic

The skip logic contains the AOI (AND OR Invert) and OAI (OR AND Invert) compound gates for skip logic. The gates, which contains of fewer transistors, have lower delay, area, and smaller power consumption contrast with those of the 2:1 multiplexer [7]. As the carry propagates through the skip logics, it becomes complemented. The structure has a lower propagation delay with less area compared with those of the existing one. While the power consumed by the AOI (or OAI) gate is smaller than that of the multiplexer. Hence, the power utilization of the proposed CI-CSKA is a slight more than that of the conventional carry skip adder.

C. Incrementation Schemes

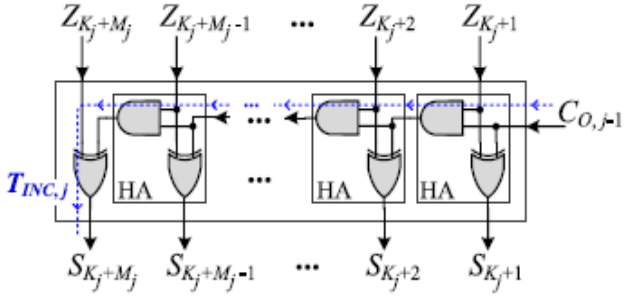

Fig. 3. Internal Structure of Incrementation Block

The internal structure of the incrementation block contains a chain of half-adders (HAs). In order to reduce the delay, the carry output of the incrementation block is not handled. The incrementation consists of AND gate and EX-OR gate. The carry input is fed into the structure and it carries out the operation like the half adder.

III. PROPOSED HYBRID CSKA

The structure of a generic variable latency adder used with the voltage scaling depending on adaptive clock stretching is explained. Then, a hybrid variable latency CSKA structure based on the CI- CSKA structure described in Section II is proposed.

A. Variable Latency Adders Relying on Adaptive Clock Stretching

The basic idea in variable latency adders is that the critical paths of the alders are activated rarely. If the critical paths are not activated, one clock period is enough for completing the operation. If the critical paths are activated, the structure allows two clock periods for finishing the operation. The slack between the longest off-critical paths and the longest critical paths is the maximum amount of the supply voltage scaling. In the variable latency adders, a predictor block, which works based on the input pattern, is required. The carry propagation path from the first stage to the N^{th} stage is the lengthy critical path (which is denoted by Long Latency Path (LLP), while the carry propagation from first stage to the $(j+m)^{th}$ stage and the carry propagation from $(j+1)^{th}$ stage to the N^{th} stage (which are referred as Short Latency Path (SLP1) and SLP2, respectively) are the longest off-critical paths.

B. Hybrid Variable Latency CSKA

For the VSS CSKA structure, we change some of the middle stages in our proposed structure with a PPA modified. The proposed hybrid CSKA structure is shown in Fig. 4 while an M_P-bit modified PPA is used for the p_{th} stage (nucleus stage). Since the nucleus stage, which has the largest size (and delay) between the stages, is present in both SLP_1 and SLP_2, substituting it by the PPA reduces the delay of the lengthy off-critical paths. The use of the fast PPA helps to increase the available slack time in the variable latency structure. The input bits of the PPA block are used in the predictor block, this block becomes parts of both SLP_1 and SLP_2.

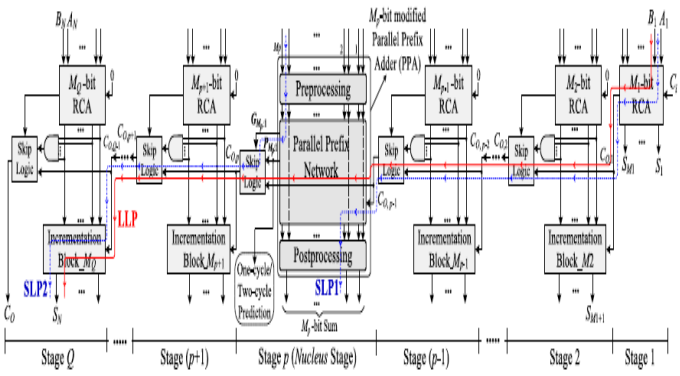

Fig. 4. Structure of the hybrid variable latency CSKA

In the proposed hybrid structure, the prefix network of the Brent–Kung adder [11] is used for constructing the nucleus stage (Fig. 5). One the advantages of the this adder compared with other prefix adders is that using forward paths, the longest carry is computed more quickly compared with the intermediate carries, which are computed by backward paths. The fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. It has a simple and regular layout. The internal structure of the stage *p*, including the modified PPA and skip logic, is shown in Fig. 5. In this figure, the size of the PPA is expected to be 8 (i.e., $M_p = 8$).

In the preprocessing level, the propagate signals (P_i) and generate signals (G_i) for the inputs are calculated. In the next level, using Brent–Kung parallel prefix network, the longest carry (i.e., $G_{8:1}$) of the prefix network along with $P_{8:1}$, which is the product of the all propagate signals of the inputs, are calculated before the other intermediate signals in this network.

The signal $P_{8:1}$ is used in the skip logic to establish if the carry output of the previous stage should be skipped or not. This signal is used as the predictor signal in the variable latency adder. Instead, when $P_{8:1}$ is zero, $C_{O,p}$ is equal to the $G_{8:1}$. Moreover, no critical path will be activated in this case. After the parallel prefix network, the intermediate carries, which are functions of $C_{O,p-1}$ and intermediate signals, are computed (Fig. 5).

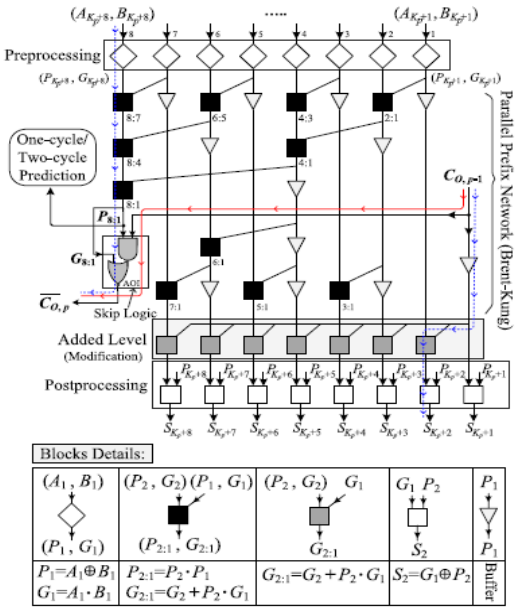

Fig. 5. Internal structure of the p^{th} stage of the hybrid variable latency CSKA.

In the post processing level, the output sums of this stage are calculated. Similar to the proposed CI-CSKA structure, the first position of SPL1 is the first input bit of the first stage, and the last position of SPL2 is the last bit of the sum output of the incrementation block of the stage *Q*. PPA structure is well-organized when its size is equal to an integer power of two. We can select a larger size for the nucleus stage.

This indicates that the third step is varied. The larger size (number of bits) leads to the decrease in the number of stages as well smaller delays for SLP1 and SLP2. The advantages of the proposed structure are lower delay, high speed, lower power delay product, lower energy delay product and low area. The applications include building blocks in Arithmetic logic units, digital signal processing, image processing, and area efficient systems like satellites, mobile phones and in battery operation based devices.

IV. RESULTS AND DISCUSSIONS

A high speed and energy efficient carry skip adder is designed and simulated successfully. In the proposed method, we could make delay, power and area reduced while comparing with earlier methods. The efficiencies of the proposed structures are done by comparing their delays, powers, energies, and areas with those of some other adders. The design proposed was developed using XILINX ISE 14.7, ModelSim and also CADENCE Virtuoso tool.

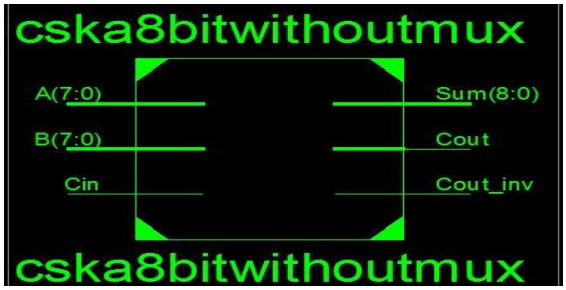

Fig. 6. RTL schematic of CI-CKSA structure.

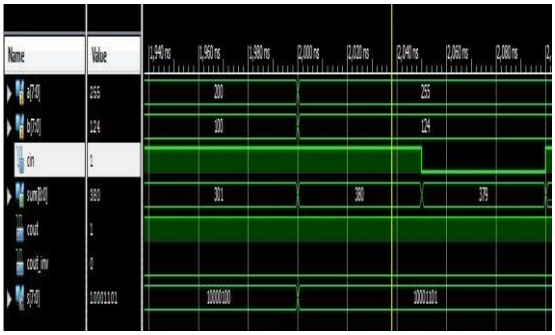

Fig. 7 Simulated output of CI-CSKA Structure

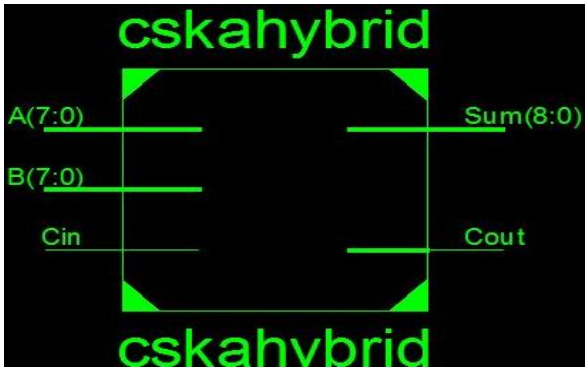

Fig. 8. RTL schematic of Hybrid CSKA

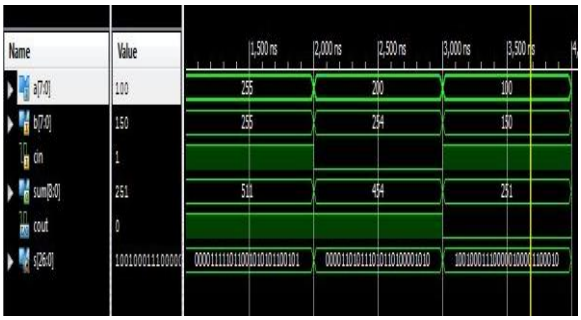

Fig 9. Simulated output of Hybrid CSKA

Figure 6 and 7 represents RTL schematic and the simulated output of CI-CSKA respectively. Figure 8 and 9 represents RTL schematic and the simulated output of Hybrid CSKA respectively. Table I represents summary details of conventional CSKA, CI-CSKA and Hybrid CSKA in terms of delay, power and area.

The result shows that CI-CSKA and hybrid CSKA has a lower delay (high speed), low power consumption and low area when compared to that of conventional one.

TABLE I SUMMARY DETAILS

CSKA: Parameter	Delay (ps)	Power (nW)	Area (μm^2)
Conventional CSKA	1388.60	92605.53	864.86
CI-CSKA	990.90	87856.17	768.40
Hybrid CSKA	699.80	76327.58	705.20

V. CONCLUSION

A simple method to increase the speed of conventional carry skip adder is done. The concatenation and incrementation technique is used to modify the structure for speed enhancement by replacing the multiplexer logic with low power gates such as AOI-OAI. The simulation result shows that the delay of the modified adder (CI-CSKA) is reduced when compared to the conventional structure. The results also suggested that the CI-CSKA structure is a very good adder for high-speed application where both the speed and energy consumption are essential. The proposed CI-CSKA is an efficient adder in terms of speed and power consumption. A hybrid variable latency extension of the structure is also proposed. It uses a modified parallel adder structure at the middle stage to increase the slack time which lowers the energy consumption. The structure gives lowest delay, power and area that is used for high-speed low-energy applications.

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