Design and Implementation of a Low-Voltage Low-Power Double-Tail Comparator

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Abstract-
In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages.Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18μm CMOS technology confirm the analysis results.

Keywords **-** Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design**.**

I. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. .

The designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve

high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods , techniques employing body-driven transistors current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architectures. Furthermore, based on the double-tail structure proposed in , a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double-tail comparator dynamic comparator and double-tail comparator. Clocked regenerative comparators have found wide applicationsin many high-speed ADCs since they can makefast decisions due to the strong positive feedback in theregenerative latch. Recently, many comprehensive analyseshave been presented, which investigate the performance ofthese comparators from different aspects, such as noise offset and , random decision errors , andkick-back noisedynamic comparator and double-tail comparator.

II. BLOCK DIAGRAM

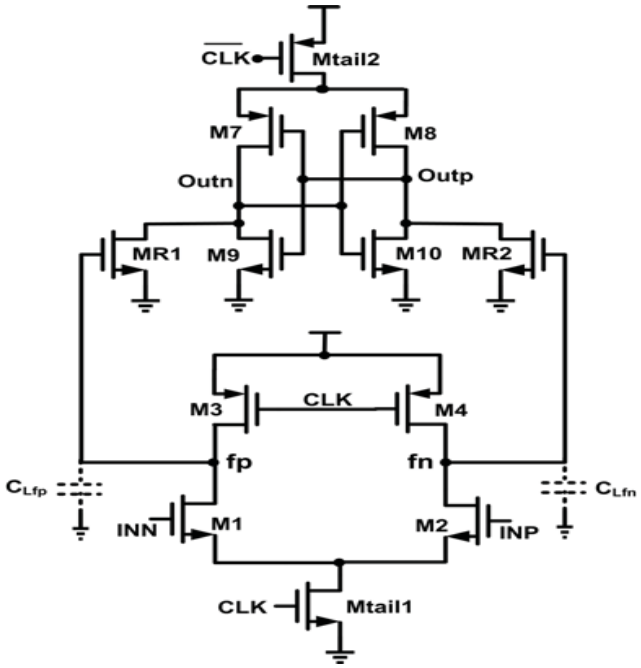

Fig.1: conventional double-tail dynamic comparator

III. DESIGN AND IMPLEMENTATION

A conventional double-tail comparator.This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset . The operation of this comparator is as follows (see Fig. 4).During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During decision-making phase (CLK =*V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1*/C*fn(p*)* and on top of this, an input-dependent differential voltage _*V*fn(p*)* will build up. The intermediatestage formed by *M*R1 and *M*R2 passes _*V*fn(p*)* to the crosscoupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise . Similar to the conventional dynamic comparator, the delayof this comparator comprises two main parts, *t*0 and *t*latch.conventional

Feature Detection using FAST

Operation of the proposed comparator

The operation of the proposed comparator . During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, avoiding static power), *M*3 and *M*4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2, reset both latch outputs toground. During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose*V*INP >*V*INN, thus fn drops faster than fp, (since *M*2 provides more current than *M*1).

.SYSTEM SOFTWARE

Tanner Software:

Today's semiconductors and electronic systems are complex that designing them would be impossible without electronic design automation (EDA). This primer provides a comprehensive overview of the electronic design process, and then describes how design teams use Cadence tools to create the best possible design in the least amount of the time.

Design Specification:

This step involved stating in definite terms the performance of the chip. Like if we are making a processor, data size, processor speed, special functions, power etc. is clearly stated at this point. Also somewhat it is decided, the way to implement the design. So, it deals with architectural part of the design at highest level possible.

HDL:

Hardware Description Language is used to run the simulations. It is very expensive to build the entire chip and then verify the performance of the architecture. Imagine if after designing a chip for a whole year, the chip fabricated, does not come even closer to the stated specifications.

Hardware description languages provide a way to implement a design without going into much architecture, simulate and verify the design output and functionality.For eg. rather than building a mux design in hardware, we can write verilog code and verify the output at higher levelof abstraction.

Tanner EDA Design Tools:

- S-edit - a schematic capture tool
- T-SPICE - the SPICE simulation engine integrated with S-edit
- W-edit - waveform formatting

Tanner Tools:

- Tanner EDA is a suite of tools for the design of integrated circuits.
- Tanner EDA is mainly used to analyze circuits at switch level & gate level.
- These are tool used to ;
  - enter schematics
  - perform SPICE simulations
  - do physical design (i.e., chip layout)
  - perform design rule checks (DRC) and layout versus schematic (LVS) checks.

S-EDIT:

- S-Edit is a powerful design capture & entry tool that can generate netlists directly usable in T-Spice simulations.
- Provides an integrated environment for editing circuits, setting up and running simulations and probing the results.
- It also provides the ability to perform SPICE simulations of the circuit
- These circuits that can be driven forward into a physical layout.

IV. IMPLEMENTATION RESULT

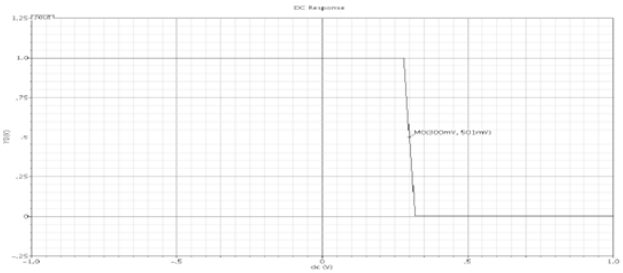

Fig.2: DC Characteristics of the comparator

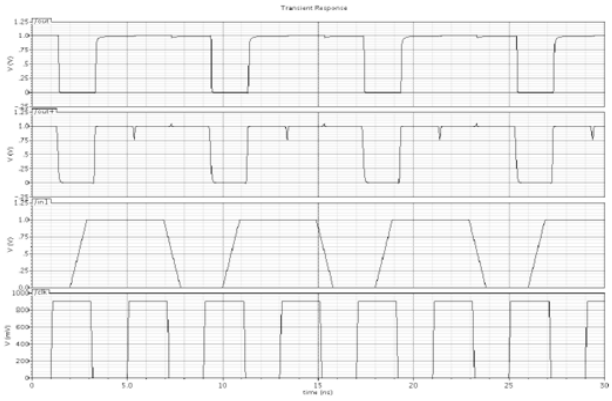

Fig.3: Transient Response of the Comparator

V. CONCULSION

The presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.The modification is power saving when compared to the conventional dynamic comparator and dual tail comparator.

VI. REFERENCE

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