Design of RRAM based Nonvolatile Lookup Table in FPGA

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Abstract - Table lookup based computation will considerably save energy consumption. Existing look up table operation strategies are measure principally utilized in ASIC styles for a few fixed functions. The goal of this paper is to change look up table computation field-programmable gate arrays (FPGAs) for prime security and instant power On.We have achieved the complete design flow to support this requirement. We propose a novel approach to build the reconfigurable lookup tables based on latest nonvolatile memories (NVMs), which takes full advantages of NVMs over conventional SRAMs and avoids the limitation of NVMs. We are introducing a new way to reduce the static power dissipation in LUT by applying DTCMOS technique. This mode gives rise to a Dynamic Threshold voltage MOSFET (DTCMOS). In DTCMOS Vt drops as gate voltage is raised, resulting in a much higher current conduction than regular MOSFET at low Vdd. On the other hand, Vt is high at Vdd = 0, thus the leakage current is low. This method is suitable for ultra low power applications.

Keywords - *Low power, FPGA- (Field Programmable Gate Array),high speed, RRAM, non-volatile SRAM (nvSRAM), DTCMOS in LUTs.*

I. INTRODUCTION

Basic NVMs, such as MRAM, PRAM,and RRAM, have better scalability and logic compatibility. As per the logic-in-memory concept, table lookup, which is the main building block in FPGAs, has been introduced with non-volatility property. Initially, nonvolatile SRAM (nvSRAM) structures with MRAM and RRAM were proposed to directly replace SRAM in the older lookup table to acquire non-volatility. The size of nvSRAM cell is much larger than that of SRAM, and the write stability is also difficult to avoid in RRAM cells. Look up Table combined with nvRRAM method has been proposed. But has more area requirement. Proposed method is a 2 input Nonvolatile memory Look Up Table for run-time reconfiguration. Third type is a DTCMOS-LUT for RRAM. In MRAM the main drawback is -Roff/Ron in less sense margin and larger area and It has larger Roff/Ron ratio. 1T1R cell has been used as the configuration bit and a reference resistor has been used to give sufficient sense margin. Single-stage amplifier is employed to reduce power and area. MRP has been added to reduce the parasitic RC mismatch between selected path in MUX and reference path for reliable sensing against logic variation, lowpower, high area efficiency, and low leakage at the same time.

Resistive Random Access Memory (RRAM)

This module consists of a traditional island-style FPGA (Field Programmable Gate Array)- fabricated in 250nm CMOS technology, on top of which the programmable resistors are integrated. Other that the configuration memory, all other parts are constructed purely with CMOS transistors. The memory array is consist with the CMOS logic throughout the tile. Write drivers, row and columns decoders and sense amplifiers are shared by the FPGA units. Memory cells are constructed using a 1T1R topology, in which programmable resistances (or PRs) behave as a voltage divider, pulling the bit line – connected to the cell through the access transistor – up or down. RRAM PRs are less in size when compared to the CMOS feature size, allowing for an optimized cell surface of only 24 F2.

FPGAs

A FPGA (Field Programmable Gate Array) is a reprogrammable integrated circuit which contains hundreds of thousands of logic gates that internally connects together to construct complex digital circuitry. There are few steps given below. It is primarily a semiconductor chip that can be configured by the user (customer or designer) after the manufacturing process has been completed. The term 'field-programmable' indicates the device is programmed by the customer, not the manufacturer. It offers certain amount of portion for re-configuration in its design.

SINGLE STAGE SENSE VOLTAGE AMPLIFIER

It has low power dissipation and a sense of basic differential amplifier in comparison to the preset voltage. The differential voltage sensing operation, provides fast loading equipment for simultaneous exchange of meaning is the primary purpose of the amplifier. SSAVC rail-to-rail voltage changes the logic

state of the resistance of the RRAM. Outb the low end and the output clock is the clock even more sense when those precharge to VDD. CLK charges the capacitor which cause waste of considerable power, as a result, when discharged to the ground. The sense amplifier may exhibit reduced clamp voltage, currents, large ROFF / RRAM Ron still without impairing the validity of the concept helps to preserve the margin.

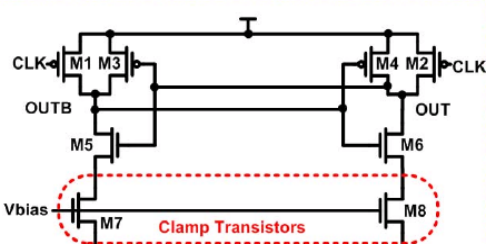

Fig 1: single stage sense voltage amplifier

Compared with the previous two-stage sense amplifier, a single-stage realization will help to reduce the area of and power as well. M7 and M8 on the gates of the clamp voltage Vbias, VDD is less than that applied to the inside of the selected nodes in the TMUX and MRP only (V bias Vth) to be precharged.

II. LITERATURE SURVEY

MRAM, PRAM, and RRAM emerging NVMs, has good quality and logic compatibility. In FPGAs the core building block of logical-memory concept, but inconsistency is there in lookup table. First, MRAM and RRAM various nonvolatile SRAM (nvSRAM) structures have been proposed to replace the volatile SRAM to achieve the classic look of the table. However, nvSRAM much larger than the cell size of the SRAM, and the writing error half of the selected disturbance RRAM cells is also difficult to avoid. For MRAM, nonvolatile two-input lookup table (nvLUT) low-power current-mode logic is based on the proposed MRAM. Also acquire sufficient sensing margin of serial / parallel magnetic junctions nvLUT proposed a six input. nvLUT proposed another MRAM-based run-time reconfiguration. LUT2 hybrid Wren proposed a third type of MRAM- based nvLUT. However, MRAM's ROFF / RON small PRAM or RRAM, the serial / parallel magnetic junctions, seems low compared to the margin, or as a result of a large area.

III. PROPOSED SYSTEM

The illustration of the proposed design, the input nvLUT presented as shown in Fig. 2. The input is all too easily be extended to six in the current mainstream FPGA products. The format of nvLUT SSAVC, a tree Multiplexer (TMUX), a MRP, a RRAM piece, and will have a footer transistor. RRAM as a reference resistor blanks at the right-most slice of the RRAM cell configuration forms for the left and four 1T1R RRAM cells.

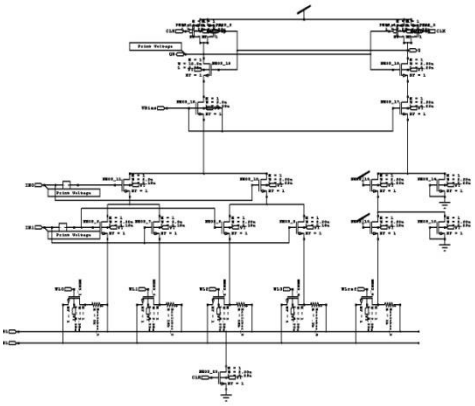

Fig2: Proposed DTCMOS based nvLUT

LOW POWER VARIATION TOLERANT nvLUT

The truth table logic voltage of SRAM is different from the resistance of the state, ROFF or RON, will be stored in the form of a piece of RRAM. For example, a NOR gate, has to program in nvLUT program, R0 RON 1, as indicated, R1, R2, and R3 ROFF represents 0. The inputs IN0 and IN1 TMUX of the RRAM cell to select the program to the program. RRT in the sense amplifier to the output 1 to be exposed to high parasitic RC bit and reference resistor, making the configuration of the memory margin between the resistance variation is subtle, reference may be slow discharge path. RRAM as a Configuration Bit and a Reference Resistor. The 1T1R RRAM cell is employed as a configuration bit and a reference resistor to provide sufficient sense margin, as shown in Fig3.

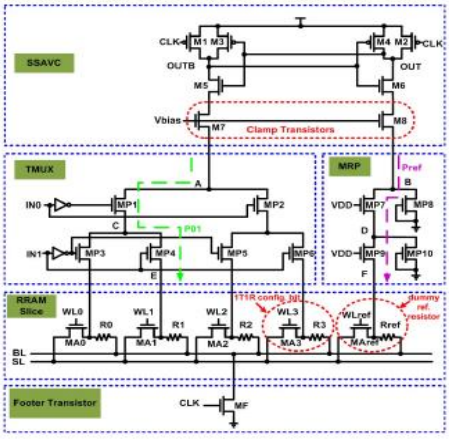

Fig3: Over all architecture nvLUT

Different from crossbar array, a 1T1R RRAM cell can eliminate the sneaking current and the disturbances during write and read, thus saving power and acquiring high yield.are of kilo-ohms and mega ohms, respectively, and ROFF/RON is over 100, which is at least 40× larger than that of MRAM. Therefore, sufficient sense margin is guaranteed and the configuration resources are also saved by half compared withthe parallel or serial combination scheme.

Moreover, the RRAM storage layer, i.e., R0-3 and Rref, is stacked in the back-end of line without occupying an additional area, as shown fig 4.Because the characteristics of RRAM are different from conventional resistor, the sense margins of RON and ROFF compared with a conventional reference resistor may suffer asymmetric changes under memory and logic process variation, which may result in read failure.

To resolve this issue, dummy RRAM cell, which is programmed to a mid state resistance, is adopted as the reference resistor. Thus, the configuration bits and reference resistor vary in the same way across different temperatures and process conditions, preserving the sense margins for both RON and ROFF. The peripheral decoding and writing circuits for dummy cell can also be shared with configuration bits, bringing less area overhead.

Single Stage Sense Voltage Amplifier It has low power dissipation and a sense of basic differential amplifier in comparison to the offset voltage. The simultaneous exchange of equipment, providing fast load-sensing operation, the sense voltage Differential is the primary purpose of the amplifier. SSAVC rail-to-rail voltage logic state changes the resistance of the RRAM. Out the low end and the output clock is the clock even more sense when the pre charge to VDD. CLK considerable power to the ground with a capacitor or waste, as a result, when the discharge level. The sense amplifier may suffer reduced clamp voltage currents, large ROFF / RRAM Ron still without impairing the validity of the concept helps to preserve the margin.

Compared with the previous two-stage sense amplifier, a single-stage realization of an area of the lower die. The clamp voltage Bias, to be implemented M7 and M8 on the gates, TMUX, MRP the selected path and the inner nodes (V bias, Vth) can only pre charged to, VDD is less than.

RRAM Slice

It constitutes of four ITIR RRAM cells at the left for configuration and a dummy RRAM cell at the right most as a reference resistor. The truth table is stored in the RRAM slice in the form of resistance state, ROFF or RON, which is different from the logic voltage in SRAM. Footer Transistor The function of footer transistor mf is to allow current to flow during sensing and it is closed during pre charge to restrain leakage.

MRP (Matched Referenced Path)

Although trimming Rref by SAWM can help to disabuse the parasitic resistance mismatch between the selected path in TMUX and reference path, their parasitic capacitance mismatch cannot be easily11 estimated and compensated. The MRP is devised to minimize the parasitic RC mismatch between the above-mentioned two paths. To illustrate this point, IN0 and IN1 are assumed to take the logic values of 0 and 1, respectively. The path marked by the green dash line in TMUX, P01, is selected to be compared with the reference path, Pref, For reliable sensing, the parasitic RCs of P01 and Pref should be equivalent. Therefore, the transistors MP8 and MP10 with their gate grounded are, respectively, added at the nodes B and D in MRP to imitate the parasitic effects of OFF-state transistors MP2 and MP3 at the nodes A and C in TMUX. Moreover, the transistors in MRP take the same size with the pass transistors in TMUX. The proposed MRP has the same parasitic RC with the selected path in TMUX, while RRT has more parasitic RC. The excessive parasitic RC in RRT may slow down the discharging of the reference path, making the sense amplifier prone to output 1 when the resistance margin between the configuration bit and the reference resistor is subtle due to memory variation.

TMUX (Tree Multiplexer)

TMUX is a multiplexer with select line in0 and in1 which are used to select the corresponding RRAM. Its working principle is similar to NOR operation.

DTCMOS

One possible solution is to use MOSFET with dynamic Vt ; it provides low Vt when the device is turned-on for high current drive, and high Vt when the device is turned-off for low subthreshold leakage.

Simulation Results and Discussions

International Technology Roadmap for Semiconductors (ITRS) identifies the key technical requirements and sets near and long term objectives for the semiconductor industry .Tanner EDA 13.0 version has used for the simulation with 250nm technology with TSMC025 process for each set of parameters .

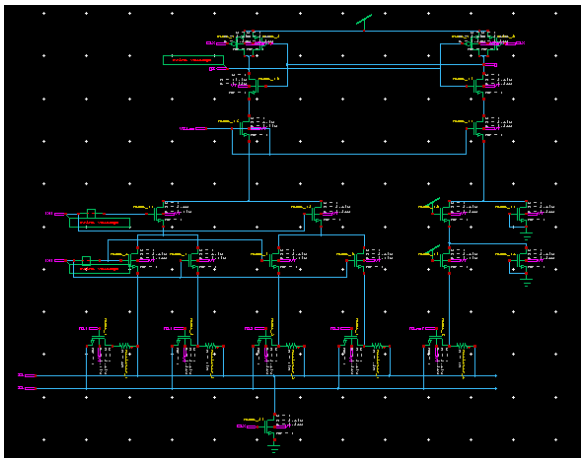

Fig.4: DTCMOS based nvLUT in Tanner

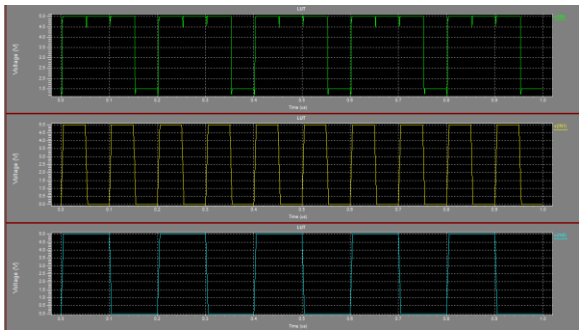

Fig.5: Waveform for XOR operation in nvLUT

Power Dissipation

The leakage current in cache memory is of major concern in deep-sub micrometer technology. The power dissipated in an RAM cell is mainly contributed by the leakage current. This is because most of the time, a major part of the memory remains idle except the row, which is accessed. Power analysis of the nvLUT has listed here with and without DTCMOS technique.

CIRCUIT	POWER DISSIPATION
nvLUT 1T1R	4.625659e-003 watts
DTCMOS based nvLUT	3.559963-003 watts

The results shows that considerable amount of power dissipation can be reduced when the circuit is designed using the DTCMOS technique. The LUT shown here is supposed to give the output of two inputs NOR gate.

V. CONCLUSION

Modern FPGAs provides various opportunity of post-fabrication reconfigurabiliy for system design. In this work demonstrates improvement of large area cost introduced by memory system of modern FPGAs. We have discussed a monolithic stacking memory with an emerging nonvolatile memory device, 1T1R. Then, we introduce peripheral circuit designs of FPGA's components, i.e. LUT, CB, and SB. At the final part, we have used CAD tools to support simulation for results. Then we have modified the circuit using DTCMOS technique which yields a larger reduction in power consumption and dissipation.

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