New Method for Quantitative Estimation and improvement of Distortion free Dynamic range of Instrumentation Amplifier

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Abstract— Research workers have suggested various methods using AC coupling networks to block undesirable DC differential offset voltages present in the input signals which get amplified by Instrumentation Amplifier (IA) reducing dynamic range at its output. However, no method of quantitative assessment and comparison of these techniques is available. Most of these methods also result into degradation of frequency response and common mode rejection ratio. Here we present a new method for quantitative estimation and improvement in Distortion free Dynamic Range of IA. We propose a new Figure of Merit called as Distortion free Dynamic Range Improvement ratio (DDIR) which takes into account the effect of DC blocking circuits on degradation of frequency response and Common mode rejection ratio (CMRR) at various frequencies along with improvement in dynamic range of Instrumentation Amplifier. Also a new method is proposed to block DC differential offset voltage without degrading frequency response and CMRR using constant current sources at the inputs of IA.

Keywords— Instrumentation amplifier, frequency response, Distortion free Dynamic Range, CMRR

I. INTRODUCTION

An instrumentation amplifier (IA) is able to amplify faithfully low level differential signals in presence of large common-mode signals and noise. Therefore it is suitable as input stage of many signal processing systems. Many times DC differential offset voltages are present in input signals which also get amplified by differential gain of IA along with useful input signals and appear as large dc voltage at its output. [1],[2],[3]. This reduces useful range of amplification of input differential signal as amplification of DC differential offset voltage may lead to saturation of IA output. [4],[5].

Several research workers have worked to solve this problem [6],[7] using R-C networks at the inputs of IA.

Fig.1 shows a typical circuit for balanced AC coupling to block the DC offset voltages. However in this configuration, CMRR is affected which depends on component tolerance and the input signal frequency and is degraded by source impedance unbalances. In this circuit, both CMRR and

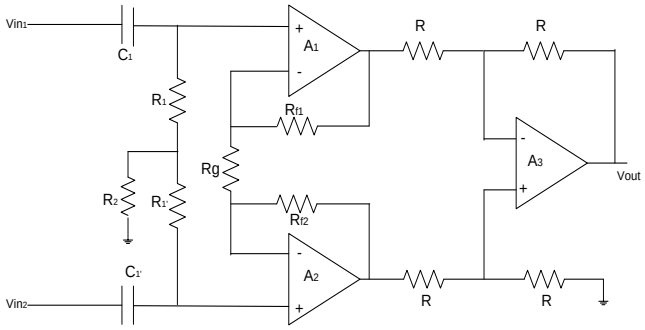

Fig 1: Typical circuit for balanced AC coupling

common mode impedance increase with R_2. However, R_2 cannot be made extremely large since the bias current flows through it, creating a large voltage drop across it which will spoil the performance of the circuit [6].

To solve these problems an alternate AC coupling circuit has been proposed without any grounding resistor as shown in Fig 2.

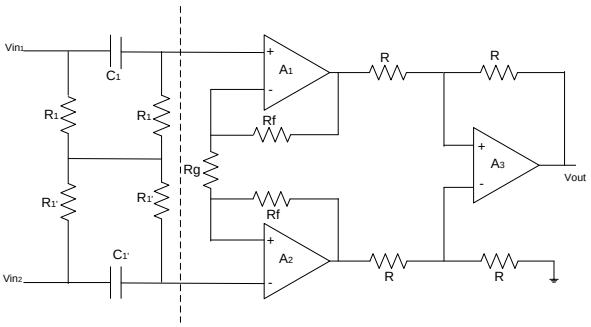

Fig 2: AC coupling circuit without any grounding resistor

In this circuit, the input network is not grounded. If a common mode input voltage is applied, potentials available at all network's nodes are same [6]. Hence high CMRR is obtained which is independent of component tolerances. However, due to unbalanced electrode impedances, CMRR is reduced. One more disadvantage of this configuration is that it requires a path for input bias current which is provided by third reference electrode in case of biosignal amplification [6]. Limitation of all AC coupling methods is that they degrade the low frequency response of IA and DC contents in input signals are also blocked, converting unipolar signal to bipolar one. Since various methods have been developed for blocking DC

differential offset voltages, there is a need to assess and compare the performance of all these methods developed for this purpose. Previous research workers have assessed the performance of their circuits based on CMRR values at different frequencies [8],[9]. However, frequency response of circuits also gets affected because of the DC blocking methods. e.g all such DC blocking networks block the DC content of input signal as well as low frequency components in the signal to some extent. Thus, there is no performance parameter or Figure Of Merit (FOM) which quantifies the effectiveness of the DC offset blocking circuit with respect to degradation of the frequency response as well as degradation of CMRR introduced by this circuit. Thus FOM is needed to assess and compare performance of various schemes.

Here, we introduce a new parameter or FOM named Distortion free Dynamic range Improvement Ratio (DDIR) and a new method to achieve high value of this FOM so that DC differential offset voltages can be blocked more effectively without affecting frequency response and CMRR.

II. NEW FIGURE OF MERIT AND CONCEPT OF DDIR

As pointed out by many research workers conventional R-C coupling circuits used for blocking DC offset voltages also block low frequency components because of which the differential gain of IA obtained using DC blocking circuits (Adcomp) is not same as Ad which is differential gain of IA without blocking network. This effect of change in Ad can be assessed by a parameter Adcm(f)/Ad(f), a ratio which is unity in ideal case but many times much less than one when R-C blocking circuits are used. Similarly due to finite tolerance of components in R-C network used at input of IA for blocking DC voltages, the AC components are attenuated to varying extent resulting into common mode gain Acmcomp for IA with blocking network which is much higher than Acm i.e common mode gain for IA. This degrade in common gain is frequency dependant and can be assessed by parameter Acm(f)/Acmcomp(f), a ratio which is one in ideal case but less than one in many applications. Finally, the method used for blocking DC offset may not be able to block or compensate the DC offset perfectly.

If V_{DR} is output of DC voltage of IA without using DC compensation technique and Voff is residual DC voltage at output of IA after use of compensation technique, the effect of imperfect DC offset compensation can be assessed by parameter (VDR-Voff)/VDR which varies from 0 to 1 and is one in case of perfect compensation. Based on these three parameters we define a FOM for DC compensated IA as DDIR.

DDIR describes the quantitative assessment of an ability of a differential amplifier to reject a differential DC offset voltage signal without affecting its frequency response and CMRR.

DDIR is given by following equation:

$$FOM = DDIR = (A_{dcomp}(f) / A_d(f)) . (A_{cm}(f) / A_{cmcomp}(f)) . ((V_{DR}-V_{of})/V_{DR}) \quad ---------(1)$$

In the above formula --

$A_d(f)$ - Differential gain of IA without using any compensation technique.

$A_{dcomp}(f)$ - Differential gain of IA after using DC blocking technique.

$A_{cm}(f)$ – Common mode gain of IA without using any compensation technique.

$A_{cmcomp}(f)$- Common mode gain of IA after using DC blocking technique.

V_{of} - The output DC voltage of IA corresponding to differential offset voltage with DC Compensation

V_{DR} – Output voltage corresponding to linear range of IA

Thus DDIR is the product of three basic factors as described above. Any DC compensation technique affects one or more of these factors degrading the DDIR. Every individual factor of all these three factors above mentioned has a range of variation from zero to one. In worst possible case, the factor is zero and best possible case it is one. Hence the value of DDIR also is zero for worst case and one for best possible case.

The best possible case is indicated when all the three factors are one. The value of one for 1st factor i.e. $(A_{dcomp}(f) / A_d(f))$ indicates that there is no degradation of the frequency response of IA due to compensation technique. The value of one for 2nd factor i.e. $(A_{cm}(f) / A_{cmcomp}(f))$ indicates that there is no degradation in common mode gain of IA at any frequency and value of one for 3rd factor indicates that DC differential offset voltage has been exactly compensated. Thus the value of one for DDIR indicates that the DC offset voltage compensation has been correctly implemented totally without any residual offset voltage and without degradation of frequency response as well as CMRR of IA. The formula gives equal weightage for all the three factors of interest i.e. 1) frequency response of IA, 2) CMRR and 3) perfect DC offset voltage compensation, since all factors vary from zero to one.

It is quite clear that for commonly used DC blocking techniques such as R-C coupling networks the $A_{dcomp}(f)$ is equal to zero for DC input signal. And for low frequency signal, $A_{dcomp}(f)$ is small as compared to $A_d(f)$ and it increases with the frequency till it becomes equal to $A_d(f)$. So the factor $(A_{dcomp}(f) / A_d(f))$ becomes unity only for higher frequencies. Hence this factor represents the distortion in the gain of IA at various frequencies which is introduced by DC blocking network.

Similarly, the factor $(A_{cm}(f) / A_{cmcomp}(f))$ represents the distortion introduced in CMRR of IA which is mainly due to the finite component tolerance of DC blocking network used for the purpose. Oscar Casas etc [9] have compared the distortion introduced in CMRR when various DC blocking networks used and they have shown that this factor depends upon the method used and is a function of the input signal frequency. For ideal system, this factor should be equal to one at all the frequencies.

Third factor $((V_{DR}-V_{of})/V_{DR})$ represents effectiveness in improving the dynamic range of output signal. When input

offset voltage is totally blocked, this factor becomes equal to one.

Factor 1 and factor 2 are less than one for DC and low frequency signals for conventional AC coupling circuits. Hence the FOM is less than one at DC and low frequencies signifying the distortion introduced in the signal amplification at DC and low frequency present in the signal.

It has been shown that in the new method, proposed in this paper, the factor 1 and 2 are equal to one and factor 3 can also be made equal to one by proper adjustments in the circuit. This method can be implemented by using constant current sources for compensation of the offset voltage over a wide dynamic range. However, for limited range of offset voltages, even constant voltage sources can be utilized without significant degradation in circuit parameters as defined above.

III. PROPOSED CIRCUIT OF DC OFFSET VOLTAGE COMPENSATION WITH CONSTANT CURRENT SOURCES

The proposed circuit describes the novel technique for compensation of unwanted DC differential offset voltage without use of R-C network. It uses current sources across Rg of Instrumentation amplifier to inject currents to compensate the current Ig flowing through Rg, Rf1and Rf2 which is produced due to DC offset voltages as shown in Fig 3. The current sources are controlled by voltages V1 and –V1 generated using inverting amplifier.

Mathematical Analysis:

Let Vo1 and Vo2 be the output voltages of amplifiers A1 and A2 respectively.

Va and Vb are the DC offset voltages present in the applied input signals Vin1 and Vin2 respectively which are applied at the non-inverting terminals of amplifiers A1 and A2.

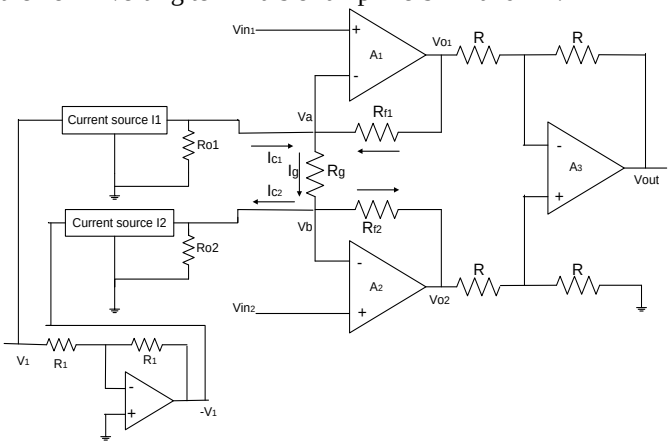

Fig 3: New method of DC offset voltage compensation with constant current sources

Since both the amplifiers A1 and A2 are working in linear region, these DC offset voltages Va and Vb will appear at their inverting terminals also. Because of this, a current Ig which flows through Rg is given by (Va-Vb)/Rg. In absence of any compensation technique, this current will also flow through Rf1and Rf2. Thus a large differential voltage (Vo1-Vo2) is created at the output of IA.

Ic1 is the current produced by current source I1, part of which flows through Rg and Rf1. The current Ic2 is the compensation current produced because of current source I2, part of which flows through Rg and Rf2. The direction of the current of Ics shown in the Fig 3 corresponds to the case when Va>Vb. It will be reversed in case when Vb>Va.

Ro1 and Ro2 are the output source impedances of current sources I_1 and I_2 respectively.

In this case,

$Vo1 = (Va-Vb)Rf1/Rg + Va\ (Rf1/Ro1) – Ic1Rf1 + Va$ ---(2)

$Vo2 = - (Va-Vb)Rf2/Rg + Vb\ (Rf2/Ro2) + Ic2Rf2 + Vb$ ----(3)

Therefore,

$(Vo1- Vo2) =(Va-Vb)\ [1+ (Rf1+ Rf2)/Rg]–Ic1\ Rf1– Ic2\ Rf2 + [Va.(Rf1/Ro1)–Vb(Rf2/Ro2)]$—(4)

The above expression for (Vo1-Vo2) includes three terms –

1) The output of IA corresponding to amplifier of uncompensated differential DC offset voltage which is given by the term as (Va-Vb) [1+ (Rf1+ Rf2)/Rg],
2) The compensating voltage produced at the output of IA corresponding to compensation currents Ic1 and Ic2 which is given by (Ic1 Rf1 + Ic2 Rf2)
3) The error voltage produced at the output of IA because of finite value of Ro1 and Ro2 which are output source impedances of constant current sources utilized for this purpose. This term is given by [Va (Rf1/Ro1) – Vb (Rf2/Ro2)]. For ideal current sources both Ro1= Ro2 = ∞. Then this 3rd term is reduced to zero. However when Ro1 and Ro2 are finite then the error due to this is decided by mismatch between ratios of Rf1/Ro1 and Rf2/Ro2.

To assess the effect of mismatch of these ratios, we examine a case when the ratios (Rf1/Ro1) and (Rf2/Ro2) have 5% mismatch i.e. when they differ by ±5% from each other.

Let Rf2/Ro2 = Rf1/Ro1 (1±0.05) then (Vo1-Vo2) becomes –

$(Vo1-Vo2) = (Va-Vb)\ [1+ (Rf1+ Rf2)/Rg] - Ic1\ Rf1– Ic2\ Rf2 + (Va-Vb)(\ Rf1/Ro1) \pm (0.05xVb\ \ (Rf1/Ro1))$

$(Vo1-Vo2) = (Va-Vb)\ [1+ (Rf1+ Rf2)/Rg + Rf1/Ro1] – Ic1Rf1 –Ic2\ \ Rf2 \pm\ (0.05\ (Vb.\ Rf1/Ro1))$

Thus error factor consists of two terms, (Va-Vb)(Rf1/Ro1) and 2nd term is ±0.05 (Vb Rf1/Ro1). The first term is very small and is proportional to (Va-Vb) and therefore does not degrade the performance of IA. However ± 0.05 (Vb. Rf1/Ro1) is the error which is not neutralized. Thus the total error is given by ± 0.05 (Vb. Rf1/Ro1) which error produced because of 5% mismatch in these ratios. It is clear that this error will reduce for higher values of Ro1, Ro2 and low values of Rf1, Rf2.

For a typical case, when Rg = 100Ω, Rf1 = Rf2= 1KΩ, differential gain is 21 and if Ro1= Ro2 are nearly 10MΩ, then Error factor = ±0.05 Vb (Rf1/Ro1)

$= (5x10^{-6})Vb$

This error is quite small. The error can be reduced further if Ro1 and Ro2 are made much larger and/or Rf1 and Rf2 are used with tight tolerances (0.1% or less). With the existing technology, it is possible to design the constant current sources with output source impedances as high as 1000MΩ using which the error can be further scaled down. In such case, the error will be reduced to very low figure which can be as small as $(5x10^{-9})$Vb .

To find the value of compensation current Ics which is required to compensate the total differential offset voltage, it is quite clear that DC offset voltage (Va-Vb) is given by the following equation. In most of the cases, Ic1=Ic2= Ic.

In this case, (Vo1 – Vo2) = 0

Hence, Ic = (Va-Vb) [1/(Rf1+ Rf2) + 1/Rg] since Ro1 and Ro2 are very large values.

The exact Dc compensation can be implemented by adjusting V1 manually using a potentiometer. Alternately an automatic adjustment of DC offset at the output but DAC based compensation can be used. For this purpose the output of IA is integrated with large time constant to extract DC component in input and this input is nullified/minimized by compensation current/voltage produced at DAC output for which the code to DAC is adjusted as shown in Fig.4. Since the amount of DC offset voltage compensation depends upon DAC code, this code is controlled during compensation phase of IA. Since the code remains fixed during application of input signal, low frequency components in input do not get affected by this compensation.

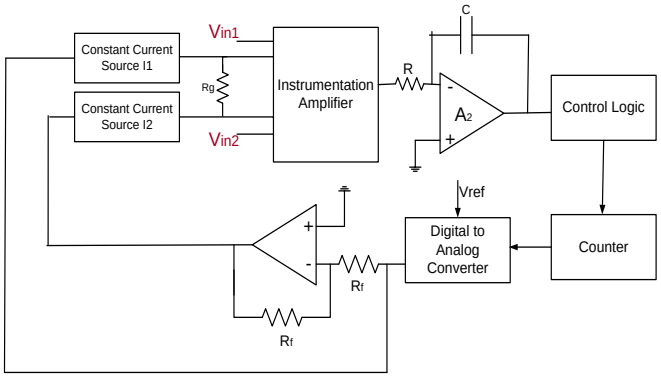

Fig 4: Instrumentation amplifier circuit with automatic offset voltage compensation

IV. RESULT

The proposed compensation circuit was simulated with Multisim software, version 12 of National Instruments. The simulation circuit is as shown in Fig 5. Here, voltage controlled current sources were used at the inputs of IA to compensate DC differential offset voltages. The circuit was tested for various DC differential and common mode signals to observe the performance of IA without compensation and with compensation of the unwanted DC offset voltages. Similarly AC common mode performance was tested with 1KHz AC common mode signal which was varied from 0 to 10V. For testing the performance of amplifier for differential input voltages, the DC differential signals as well as AC differential signals were applied at the input and output was observed. To see the effect of compensation, the DC voltage was added with AC signal at the input of IA and its performance was observed for such composite input signals. The observations were made using the matched components i.e Ro1=Ro2 and Rf1= Rf2 for assessing the performance with ideal compensation conditions. To verify the performance due to mismatch in ratios of Rf1/Ro1 and Rf2/Ro2, the value of Ro2 was taken 5% different from Ro1 to represent tolerance. These observations were carried out under conditions of 1) without compensation of offset voltage 2) compensation of offset voltage with matched components of current sources (Ro1, Ro2) and 3) compensation of offset voltage with mismatch components of current sources. The observations under all these cases were made for DC differential and AC differential signals as well as DC and AC common mode signals. The graphs under various conditions were plotted to compare the performance and find out the efficacy of the new method which has been proposed here—

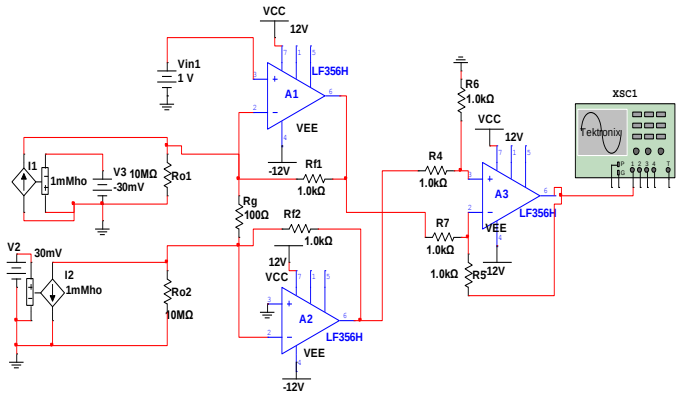

Fig 5: Simulation Circuit of proposed scheme

Simulation results:

The graph in Fig 6 is plotted for DC differential input signal ranging from 0-4 mV without compensation of offset voltage as well as with compensation using Ro1 = Ro2 =10MΩ, Rf1 = Rf2 = 1KΩ.

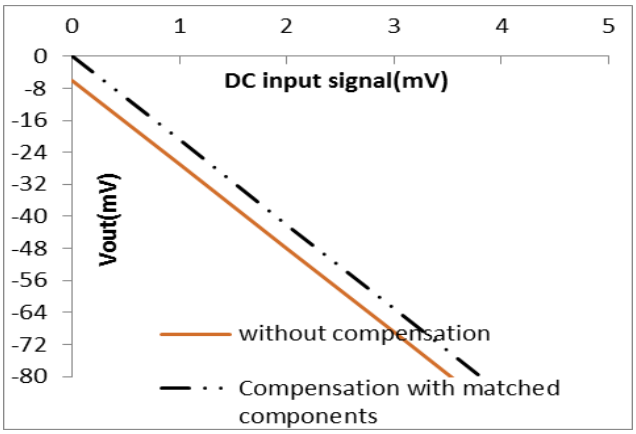

Fig 6: Performance of IA for DC differential input signal

It is quite clear from the above graph that for uncompensated offset voltage, -6mV DC is observed at the output for DC differential voltage of 0mV. For compensated circuit, the output is 0mV for same input and the output is proportional to input differential voltage in both the conditions. Thus in this method, the DC differential voltage is amplified faithfully unlike other methods which are used for blocking DC differential offset voltages.

Fig 7 shows the graph when compensation is done using 5% mismatch i.e Ro1 = 10MΩ, Ro2=9.5MΩ, Rf1 = Rf2= 1KΩ. As discussed earlier, the error produced due to mismatch is in the range of microvolts and hence both the graphs with ideal and non-ideal compensation practically track each other.

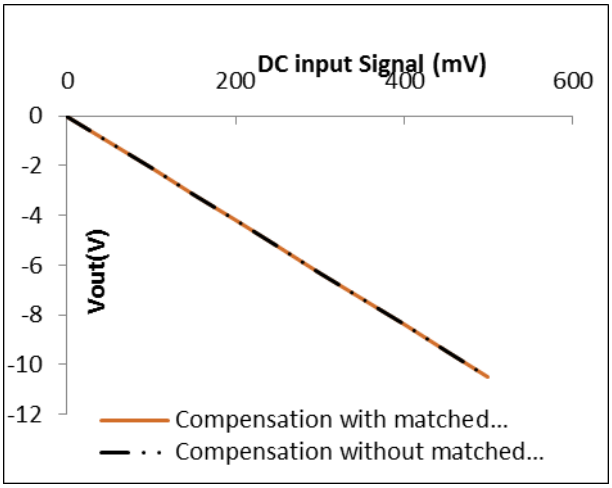

Fig 7: Performance of IA for DC Differential input with compensation with and without matched components

The graph in Fig 8 gives the common mode performance of IA for DC input voltage ranging from 0-8V. Here, without compensation the output is always -6mV whereas with compensation the output is zero.

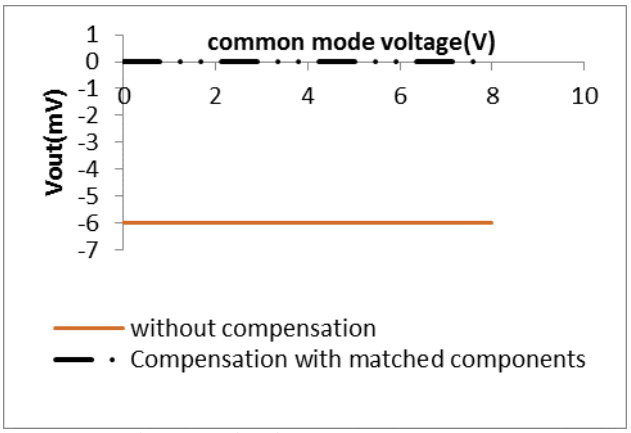

Fig 8: Performance of IA for common mode DC input signals

Fig. 9 shows the performance of IA for common mode input ranging from 0-8V DC. It is clear from the graph that the common mode error introduced for 5% mismatch the common mode voltage is maximum nearly 40µV which is quite small.

Fig 10 and 11 show frequency response of IA for differential AC input signals without compensation and with compensation using matched and mismatch in components. As expected, both the graphs give the same frequency response without any distortion for AC input voltage of 2.8mVpp for all the frequencies.

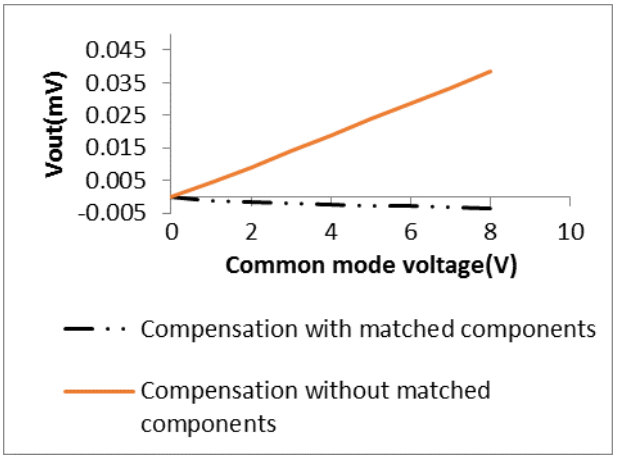

Fig 9: Performance of IA for DC common mode input with compensation with and without matched components

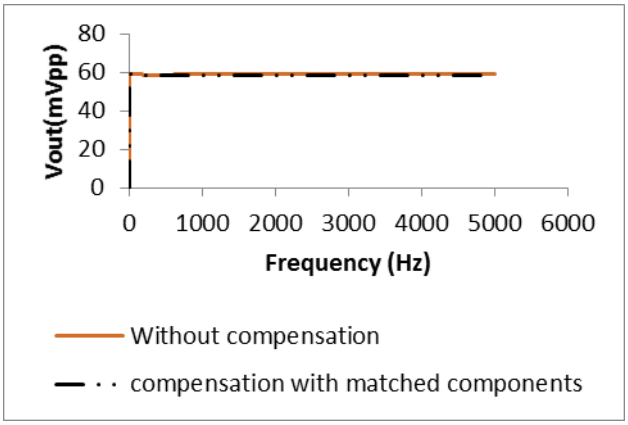

Fig 10: Frequency response for Differential AC input signals

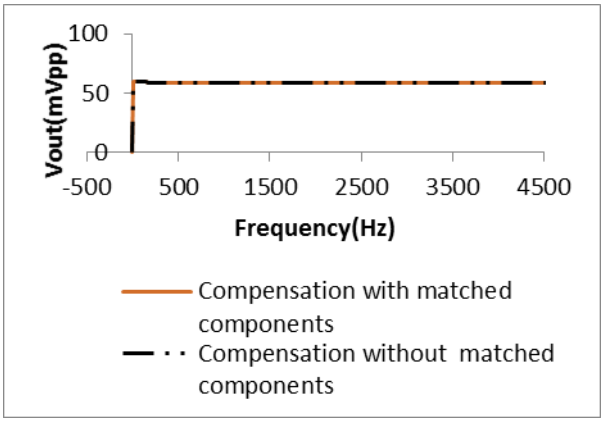

Fig 11: Frequency response for differential AC input signals using compensation with and without matched components

Fig 12 and 13 show the response of IA for common mode AC voltage of 1KHz from 0-8Vpp. It can be seen that the output is in the range of few hundreds of micro volts which is nearly the same as it is in case of circuit without compensation and in ideal and non-ideal compensation. Hence the proposed method has negligible effect on the CMRR.

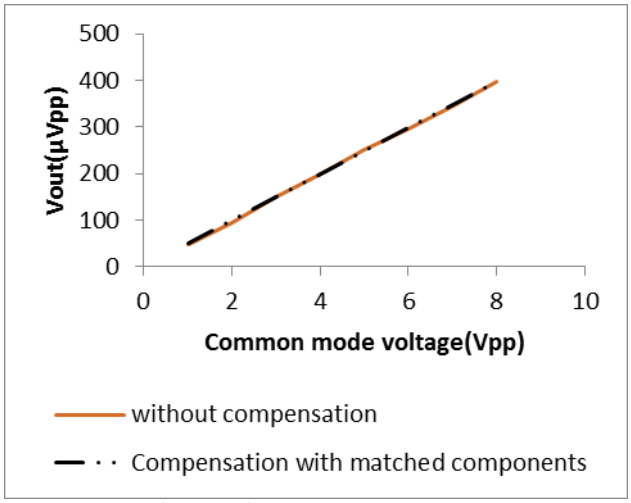

Fig 12: Performance for Common mode 1KHz AC input voltage

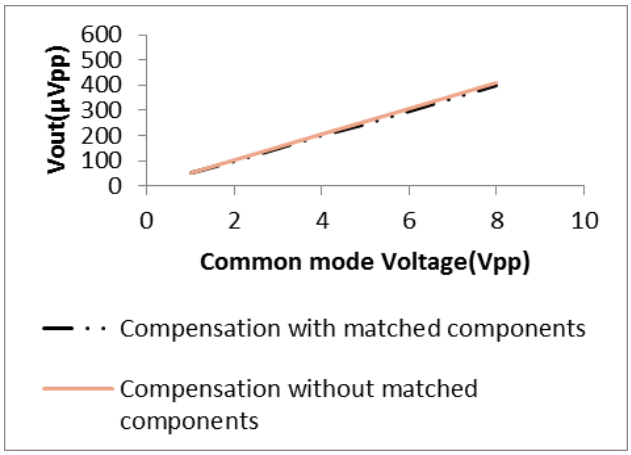

Fig 13: Performance for Common mode 1KHz AC input voltage with compensation with and without matched components

Graphs shown in Fig 14, 15, 16 have been plotted with composite signals applied at the input of IA. Fig 14 shows output corresponding to 2mVpp AC signal superimposed over 500mV DC input. These graphs illustrate the improvement in dynamic range. For uncompensated DC input of 500mV, the output is saturated at -10V and therefore AC signal applied along with DC input leads the saturation of IA and zero AC output is produced at all frequencies which is in the case of graphs 14 and 15. When the compensation is done, the saturation is totally avoided producing zero output for DC which indicates that dynamic range has been improved by 10V. The AC signal is faithfully amplified here at all frequencies resulting into flat frequency response and uniform gain. As shown in Fig 15, for compensated circuit the AC input voltage of 50mVPP is also amplified faithfully resulting into uniform frequency response.

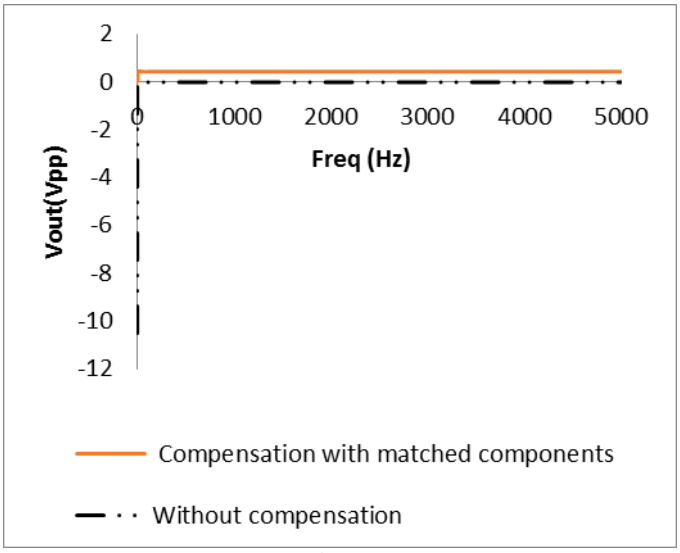

Fig 14: Frequency response for 2mVpp AC+500mV DC input

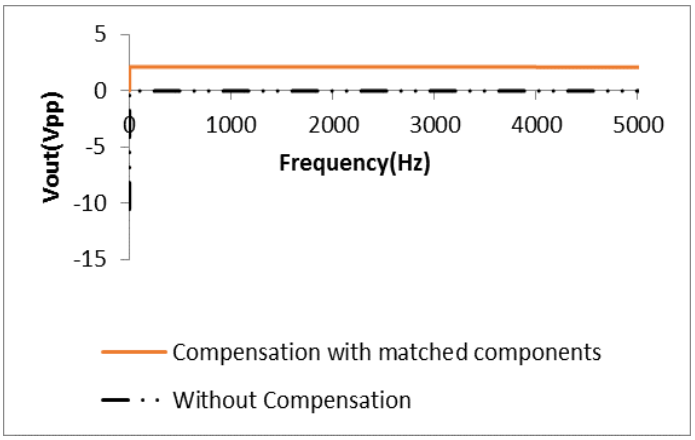

Fig 15: Frequency response for 50mVpp AC+500mV DC input

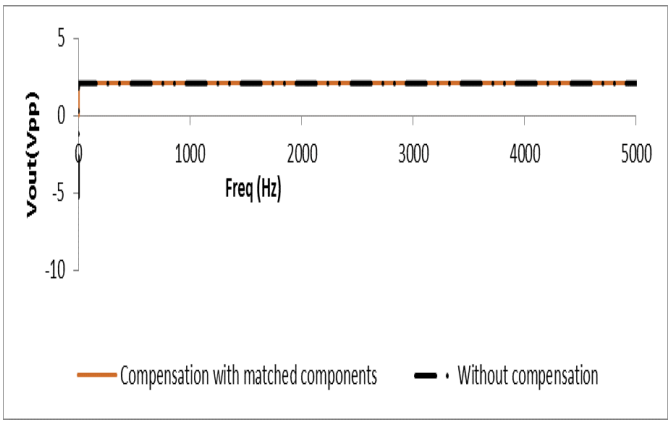

Fig 16: Frequency response for 50mVpp AC+250mV DC input

Fig 16 illustrates the case where DC voltage of 250mV is applied along with 50mVpp AC at various frequencies.

For uncompensated circuit, the output voltage is nearly -5.26V for DC signal and application of 50mVpp signal does not saturate the IA as in previous case. The output of IA is nearly 2V at all the frequencies. The compensated output matches with this frequency response. However, the DC output of IA is zero in this case indicating distortion free dynamic range has been improved by 5V.

It should be noted here that for illustration of the effects of errors due to the mismatch of Ro1, Ro2, Rf1 and Rf2 the smaller vales of Ro1 and Ro2 were selected which are nearly equal to 10MΩ. However it is possible to make Ro1 and Ro2 as high as 1000MΩ and also to select Rf1 and Rf2 with 0.1% tolerance. Using such values, the errors due to mismatch of the components will be scaled down to nearly 1% of whatever has been illustrated here.

V. CONCLUSION

This paper proposes a new method for quantitative assessment of efficacy in improvement of distortion free dynamic range of IA using a new parameter, Figure of Merit (FOM) named Distortion free Dynamic range Improvement Ratio (DDIR). Various methods suggested by research workers result into distortion of frequency response and CMRR at lower frequencies including DC. These methods give significantly small value of DDIR at low frequencies. For best possible compensation technique, this ratio should be equal to one at all frequencies. The new method of compensation of DC differential voltage can give this FOM nearly equal to one indicating the improvement in dynamic range without introducing distortion in frequency response and CMRR of IA at various frequencies.

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