Design of Low Power 128 Kb CMOS Josephson Hybrid Memory Using Single Ended 8T SRAM

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Abstract- In this paper we design a 128 kb CMOS Josephson Hybrid Memory. To overthrown a memory bottleneck in Single Flux Quantum digital system. To achieve larger scale and higher speed Single Flux quantum circuit, aimed for reducing the power consumption of 128kb CMOS Josephson Hybrid memory system. SRAM memory system is being developed using hybrid high speed interface circuit. The whole structure of the memory is composed of Josephson Latching driver (JLD or Josephson interface circuit), CMOS differential amplifier, Binary tree decoder, memory cell (Single ended 8T SRAM) , Level driven DC/SFQ converter (Josephson current sensor or LDDS) .128 kb CMOS memory is designed using single ended 8T SRAM. In this 8T SRAM transmission gate is used at read operation to reduce the leakage power. By using this technique low power consumption is obtained in read operation. By using this power consumption reduced and leakage power also reduced. Power consumption of 128 kb in write operation is 21.5 pWatt and read operation is 3.2pWatt.

Index Terms– *Single Ended 8T SRAM ; Josephson latching driver, Differential amplifier ; CMOS decoder; Level driven DC/SFQ Converter; SFQ Converter.*

I. INTRODUCTION

In VLSI technology the most understood memory is Static random access memory cell among all memory cells. Here nonstop advancement is going for best working of Static arbitrary access memory cell. SRAM cells are happening in various kinds in the writing like 3T, 6T, 7T, 8T. 9T, 10T Static random access cell.etc. In advanced frameworks usually SRAM cell is utilized, however in 6Transistor SRAM cell is for the most part valuable among others. 6T cell has less solidness in equivalent with the 8T SRAM. 6T SRAM configuration have two appended inverters are associated. The put away information can be in hooked these two inverters. SRAM cell having two principle activities that are perused task and compose activity. Compose task implies procedure of putting away information and the read activity implies procedure of recouping information. Compose activity as called transferring the substance in the SRAM cell and keeping in mind that bringing the substance to memory called read task. Single flux quantum has needed fast and expansive memory.

In the hybrid memory system, a fast, low power interface circuit is critical. But the difference in energy and voltage levels between signals in single flux quantum (SFQ) logic and those in semiconductor (including CMOS) circuits present a challenge for the design of high speed interface amplifiers[1]. Although the technology is mature enough, traditional semiconductor amplifiers cannot meet both speed and low power consumption requirements [4]. In the proposed venture the memory display design must be done with using of Single ended 8T Static RAM. Single completed 8T Static RAM cell, to diminish the power usage and decrease the Leakage streams. Which have transmission door procedure to diminish the power usage. This system states of the transistors which are overlooked in the midst of charging the yield from 0 to VDD. The power use is reducing as stand out from the 8T SRAM. 128 kb memory array is made using single ended 8T SRAM circuit has been differentiate and the 64 kb memory exhibit is planned using 8T static RAM.

II. 128 KB CMOS JOSEPHSON HYBRID MEMORY

A. Organization of the 128 kb hybrid Memory

The core of system is a 128 kb CMOS static random access memory (SRAM) which is designed professionally in 45nm CMOS technology to achieve minimum delay and power consumption, taking account of the 4 k properties of CMOS devices and circuits[2]. There is a high level of perfection in fabrication so one can expect that if one cell works, all cells will work. This has allowed us to make a 128 kb memory and will facilitate scaling to larger capacities a key part of memory system is the amplification of the millivolt superconductor logic signals to 60 mV using Suzuki stack (SS). Josephson latching drives a very sensitive CMOS comparator to produce the required volt level signals. The selected memory cell provides an output current that drives a superconductor detector. The main design aspects for this project are memory capacity, read access time and read power consumption. The present results of simulation and measurements on a fully functional 128 kb memory operating at 4K as well as values of access time and power dissipation. This 128 kb memory is the first fully functional 4 K memory of capacity beyond 4 Kb [5].

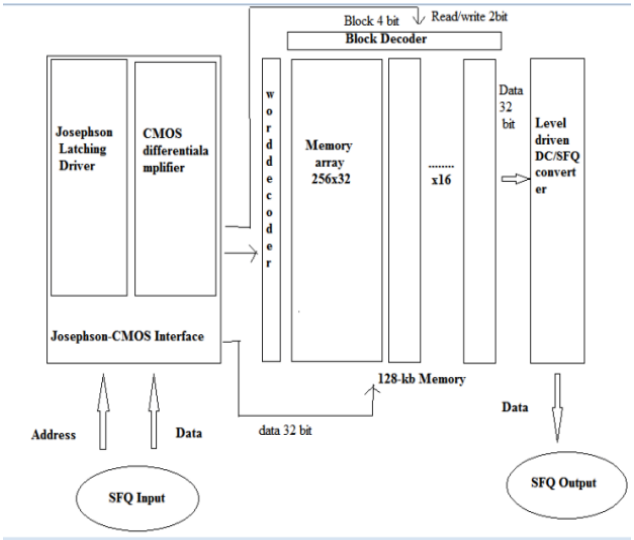

Fig.1: Block diagram of 128 kb Josephson CMOS hybrid memory system

Fig 1 shows the Block diagram of 128kb Josephson CMOS hybrid memory system. The 128 kb CMOS Josephson hybrid memory. The hybrid memory system is composed of Josephson CMOS interface circuits, CMOS memory cell array with using of single ended 8T SRAM and Josephson current sensors named as level driven DC/SFQ converter (LDDS). The CMOS memory cell array consists of sixteen blocks of 256x32 bit memory cells, where 32-bit data are written and read out at the same time. [6]

B. Josephson latching driver

Fig 2 shows the Schematic of Josephson Latching driver[20]. The driver consists of parallel 8 junction stacks[19]. Shunt resistors are added to the junctions composing the stacks to decrease the McCumber parameter bc and to achieve the high speed operation. The junction of the stack at the input part is replaced with a 2 junction SQUID gate, which increases the sensitivity of the driver to the SFQ input. Where the input data frequency is 10 GHz. One can see that the output voltage larger than 10 mV is obtained in the simulation. We have used the Josephson circuit simulator, WR spice, in the simulation of waveforms of the latching driver. We assumed the critical current density of the Josephson junction to be 2.5 kA/cm2.Operating temperature is 4.2 K [15].

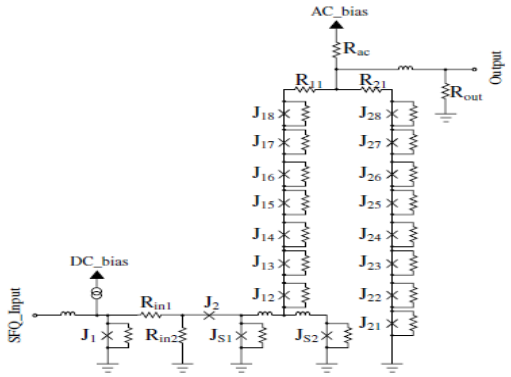

Fig 2 Schematic of Josephson latching driver

C. CMOS Differential Amplifier:

A schematic of the CMOS differential amplifier is shown in fig 3 This amplifier is composed of a self biased differential source follower in the first stage and self biased differential amplifier in the second stage. The source follower shifts the small input voltage to a certain voltage level appropriate to the second amplifier stage. A shift voltage can be controlled by the bias voltage Vbias. This CMOS differential amplifier has High immunity to process variations compared with CMOS amplifiers without self-biased architecture. It is suitable for the interface circuit in terms of the speed, power consumption and robustness[15]. an alternative idea is the utilization of nanocrytron (ntron) devices[16] as a voltage amplifier, which may achieve drastic reduction in power consumption of the Josephson CMOS interface circuit with short access time[17].

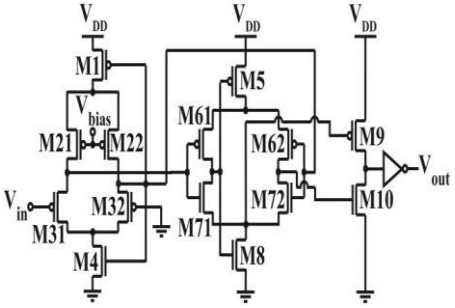

Fig 3 Schematic of the CMOS Differential Amplifier

The transistor widths are M1, M21-M32, M4, M5 M61-M62,M71-M72, M8, M9 and M10 are 12.60 um,10.72um, 9.12um,7.20um, 8.76um, 9.12um, 1.44um,4.08um,0.60um,and 0.46um respectively.

D. Single ended 8T SRAM Memory cell:

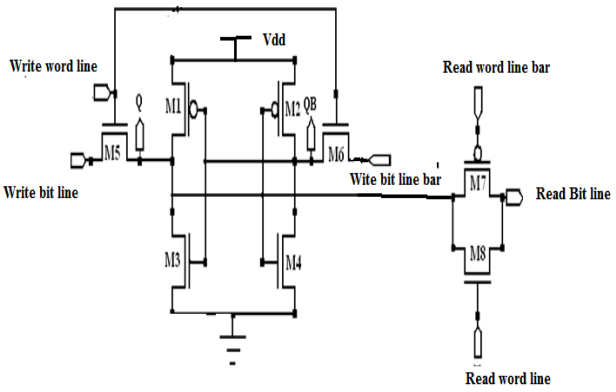

Fig.4: Schematic of Single ended 8T SRAM Memory cell

The current outline Cell is being differentiated and the single completed 8T SRAM design as showed up in Figure 4 that redesigns data unfaltering quality by improving the read Static Noise Margin and besides diminishes the power Consumption. In this plan, a transmission entryway is utilized for investigated reason. The extra standard RWLB is a reversal flag of read word line (RWL). It controls the extra transistor M7 of the transmission portal. While the

RWL and RWLB are reported and once the transmission passage is ON, a set away focus point is connected with RBL. As needs be a set away an inspiring power at Q is being exchanged to or analyzed RBL. One of the basic perfect states of this graph is that it isn't fundamental to set up a pre charge circuit as required in before 8T SRAM (static flighty access memory) cell and a sense intensifier circuit as required in 6T SRAM CELL in light of the way that the set away respect is plainly experienced transmission portal. A release/charge control on the RBL is eaten up precisely when the RBL is changed .Consequently, no power is scattered on the RBL if planned information is the same as the past state. The diagram diminishes a bit line control in the two cases that the consecutive "0"s and ceaseless "1"s are examined out [10].

E. CMOS Binary tree decoder:

Employed binary tree architecture to decrease the power consumption of the decoder. Fig 5 shows a schematic of the binary tree decoder, which is an example of a 4 bit version. The binary tree decoder is composed of one- to-two de multiplexers, switch an input enable signal to one of two output terminals depending on the Address signals. When "Address= 0", the enable signal propagates upward, and vice versa. Compared with our previous decoder, which utilizes a conventional architecture based on an array of multiple input AND gates, the binary tree decoder has power consumption due to the reduced size of buffers that drive the address lines. For example, a signal line for "Address 1" is only connected with one de multiplexer.

Power consumption is further reduced thanks to the decrease in the number of logic gates. The performance of 8 bit decoders based on the binary tree and conventional architectures[18]. We obtained about a 24% reduction in terms of the power consumption in the binary tree decoder. However, the access time was deteriorated by 185 ps due to the increase of logic stages. This is about 21%, so the tree decoder saves 24% power but is 21% slower.

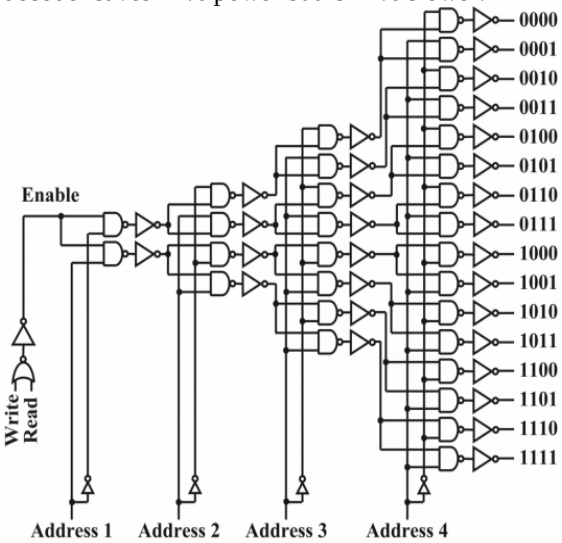

Fig.5: Schematic of the Binary tree decoder

F. Level Driven DC/SFQ converter (LDDS)

Schematic of the level driven DC/SFQ converter (LDDS) is appeared in fig 6.It works as a NRZ/RZ converter to intercede the rationale x flag qualification among SFQ and CMOS circuits. Considering the data present as an inclination source to the SQUID circle made out of J1 L2, L3, L4 and J2 the LDDS can be seen as a SQUID indicator with a JTL.

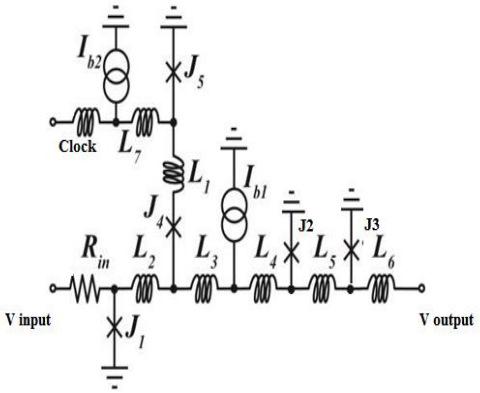

Fig.6: Schematic of the Josephson current sensor (level driven DC/SFQ converter)

The clock is originating from the SFQ input terminal, the SQUID one-sided by the information current perceives the SFQ, SFQ gives the terminal "output"[11].

III. IMPLEMENTAION OF 128 KB CMOS JOSEPHSON HYBRID MEMORY USING 8T SRAM

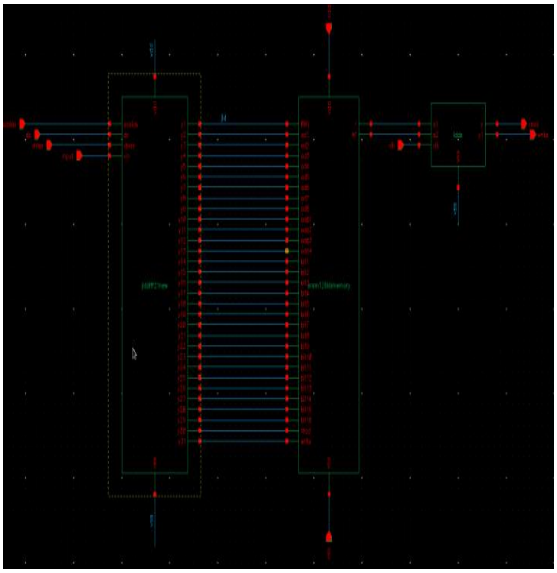

Fig.7: Schematic of 128 kb CMOS Josephson hybrid memory using single ended 8T SRAM

We are implemented and measured the 128 kb CMOS Josephson hybrid memory in virtuoso tool by using 45 nm technology which is shown in figure 7. The low power 128 kb CMOS Static RAM was attached with JLDs and LDDSs. We are implemented 31 bit Josephson CMOS interface

circuits and 16 bit LDDS circuit. The 31 interface circuits were used an 8 address lines , 2 bit control signals for read/write, 4 bit block address and 16 bit input data. In this measurement, 2 bit write/read control signals and data inputs were applied to the CMOS static RAM directly through the CMOS differential amplifiers, select address lines using binary tree decoders of memory array which designed by using single ended 8T SRAM. We have confirmed the correct memory function for all memory addresses. In figure 8 shows input and output waveforms of 128 kb CMOS Josephson hybrid memory using single ended 8T SRAM.

IV. SIMUTATION RESULTS

We achieved low power as compared to the 8T SRAM. Power consumption of Single ended 8T memory cell in write operation is 21.5 pWatt and read operation is 3.2pWatt.

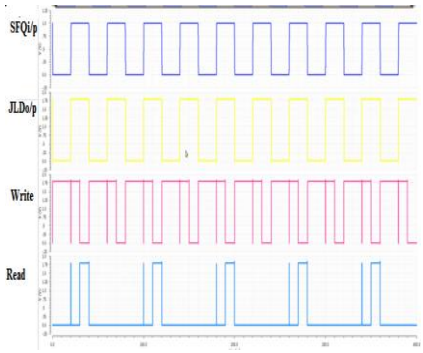

Fig.8: Waveform of 128 kb CMOS Josephson Hybrid memory system using single ended 8T SRAM

The performance comparison table 1 is shows the less power consumption between 64kb and 128 kb hybrid memory because transmission gate technique. The power consumption was estimated to be 1.84mWatt in Write operation and 1.68mWatt in Read operation in circuit simulations.

64 Kb CMOS Josephson hybrid memory using 8T SRAM					128Kb CMOS Josephson hybrid memory using single ended 8T SRAM			
Power consumption(uW)					Power consumption(uW)			
180nm			45nm		180nm		45nm	
	Read	Write	Read	Write	Read	Write	Read	Write
JLD	887.6	887.6	579	579	887.6	887.6	579	579
CMOS Amplifier	789.7	944.1	15	15.8	789.7	944.1	0.00113	0.001137
CMOS Decoder	3.816	3.77	0.000481	0.000045	3.816	3.77	0.000481	0.000045
Memory cell	5.9	5.08	0.000043	0.000139	0.349	0.465	0.0000032	0.000025
LDDS	6.2	6.2	6.19	6.19	6.2	6.2	6.19	6.19
Total	1693.216	1846.75	600.19	600.99	1687.665	1842.13	585.19	585.29

Table.1: Performance comparison of 64kb and 128 kb CMOS Josephson hybrid memory

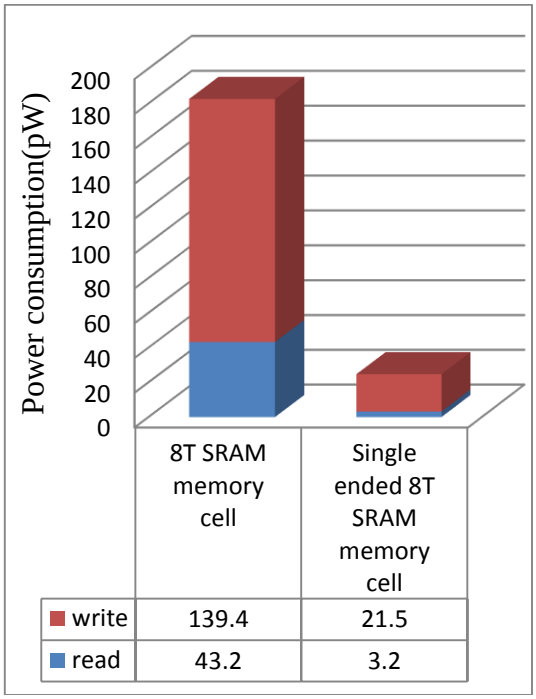

Fig.9: The power consumption chart for 64kb and 128 kb SRAM Memory cell

V. CONCLUSION

In this project, the design of 128 kb CMOS Josephson hybrid memory system is proposed to reduce the power consumption and reduce the leakage power in the read operation. The design is validated using virtuoso and ADE L Tools in the cadence EDA software.

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