An Improved Design of Brent Kung Adder Logic Using Speculation Logic

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***Abstract*—** VLSI design methodologies are increasing every day with various applications. Main module in VLSI designs are focusing the adder logic, here the parallel prefix adder is used. Carry Speculative Adder (CSA) circuit is proposed with low power consumption and reduced delay. The design step includes partitioning the adder into non-overlapped summation blocks. A parallel-prefix and carry propagate adders is obtained from structural blocks. Based on input operands the carry output of each block is determined. Here this approach taken the Brent Kung Adder proposed with speculation approach. Logic operations are used to reduce delay and the circuit uses less area. It consumes maximum depth and less area. The carry chain is reduced to two blocks and average delay can be calculated. To improve the accuracy and to tolerate error, error detection and recovery mechanism is used. Carry Speculative Adder possesses low delay, area and better output quality. The simulation results show that the CSA combined with BKA is more efficient compared with other adder logics. The performance is done by Xilinx ISE 14.2 tool and VLSI design performances of power, area, and delay results.

Keywords- *Brent kung adder; Speculation; Carry speculation adder; parallel prefix adder; Carry propagation adder;*

I. INTRODUCTION

In electronics, addition of the binary numbers in various computers and other types of processors are performed by the adders. Adder circuits are used in various processors for calculating increment or decrement operations, table indices, addresses etc. The power consumption reduction and speed improvement are the key goals in the design of digital circuit are general. One of the approaches to improve both the power and speed is to approximate adders. Adder blocks, which are the main components in arithmetic units of DSP systems, are power hungry and often from hotspots locationson the die. Prior researches on approximate adders have taken two general approaches of focusing on error weight and error probability reduction. Reducing the error probability of the summation as well as reducing the power and delay is the key design criteria. They may also accompanied by an error correction unit which has time, power and area overheads. Approximate arithmetic units are mainly based on the simplification of the arithmetic unit circuit. Different structures for approximate adders are fully approximate and only be utilized in error resilient applications. Here, by reducing the quality, the total computation time and/or power consumption of the unit is reduced resulting in higher energy degradation. The main reason behind this is that in binary arithmetic, adders are the main component to perform mathematical operations and it can perform increment, decrement, and many similar operations. The adder approximation has greater demand as the delay and power of adders increase rapidly with bit-width. Consequently, at a micro architecture level of abstraction, adders have become the key delay/power bottleneck of digital systems. One possible way to overcome this situation is to approximate adders for minimizing delay and power ignoring the accuracy. In some applications such as image processing or audio/video compression, the required accuracy might vary during run time. To runtime accuracy adjustment is obtained with a series of designs to implement accuracy, configurable approximation can be reconfigured to save more power .A new carry-prediction based configurable adder uses simple design. Simple accuracy configurable adder inherits the advantages of all previous carry- prediction-based approaches: no error correction overhead, no data stall, and allowing graceful degradation.

This paper is summarized as follows. Section 2 discussed various literature works, and section 3 proposed the speculation based BKA logic with CSA. Section 4 presents the result discussion and performance analysis. Section 5 concluded the proposed work and future possibilities.

II. RELATED WORKS

M.Lavanya and K. Rama Krishna presented the design of low power 16-bit novel carry select adder using 0.18um technology. An appropriate approach is designed in this paper to reduce the area and power of 16-bit novel CSLA. The reduced number of gates of this work provides reduction of space and energy consumption. The comparison results show that the area and power of 16-bit novel CSLA are significantly reduced by 62% and 27% respectively. The 16-bit CSLA architecture by sharing common Boolean logic term is designed to increase the performance of VLSI hardware implementation in further work.

Honglan, et al. reviewed the comparative evaluations of approximate arithmetic circuit. Often as the most important arithmetic modules in a processor, adders, multipliers and dividers determine the performance and the energy efficiency of many computing task. The demand of higher speed and power efficiency, as well as feature of error resilience in many applications (e.g, multimedia, recognition and data analytics), have driven thedevelopment of approximate arithmetic design. A comprehensive and comparative evaluation of their error and circuit characteristics is perform for understanding the features of various designs. This circuit used in image processing applications consumes as little as 47% of the power and 36% of power-delay product of an accurate design while achieving a similar image processing quality. Improvement in delay, power and area are obtained for the detection of differences in image by using approximate dividers.

III. PROPOSED METHODOLOGY

Speculation adders are designed with variable latency that combines speculation technique along with correction methodology to attain high performance in terms of low area overhead over the existing adders. In speculative adders sum and carry part is separated to reduce the area overhead. Carry speculative adder (CSPA) uses carry predictor circuit to reduce power consumption and to reduce the computational time and it uses error recognition and error correction circuit to find the fault occurred in the partial sum generator and to recover it to get accurate results.

A. SPECULATIVE CARRY SELECT ADDER

Carry chain in the addition process is observed for the design of speculative carry select addition)SCSA). The carry chain is observed because the long carry chain is rarely activated in the block adders. To overcome this problem, in SCSA the input bits are divided into two parts of equal sizes. A group of consecutive input bits are given as an input to a single block adder. A block adder is known as the window, the number of consecutive input bits is known as window size and it is denoted by K number of windows to be used is found by M=N/K where, n is the totalnumber of input bits decimal (BCD) and gray code can be added using the adder circuits.

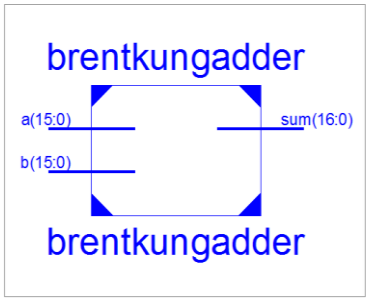


Figure1. RTL schematic view of Brent Kung adder

Adder found wide range of applications in many fields and for many operations such as decoding, calculation etc. The critical path is not often activated in traditional adders, based on this observation speculative adders have been designed. Traditional adders depend on its precious values for its each output. Particularly, the MSB of the sum depends on all the n bit previous outputs, where n is the blockadder width. As the width of block adder increases, there will be an error growth. The error grows linearly with n. there willbe a large area and large fan out at the primary inputs due to this error.

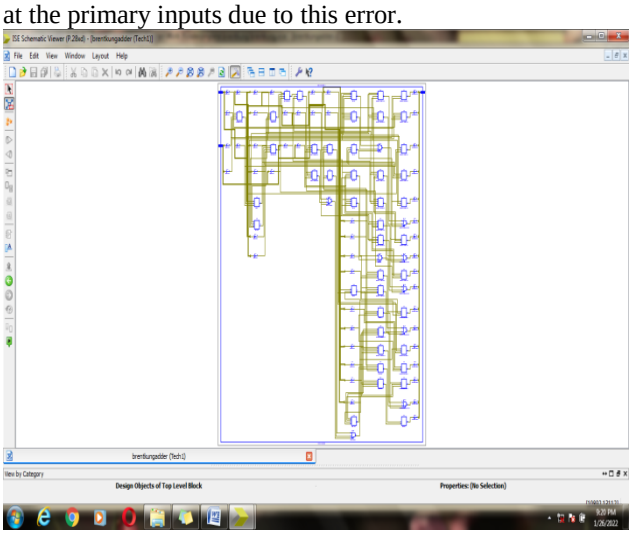


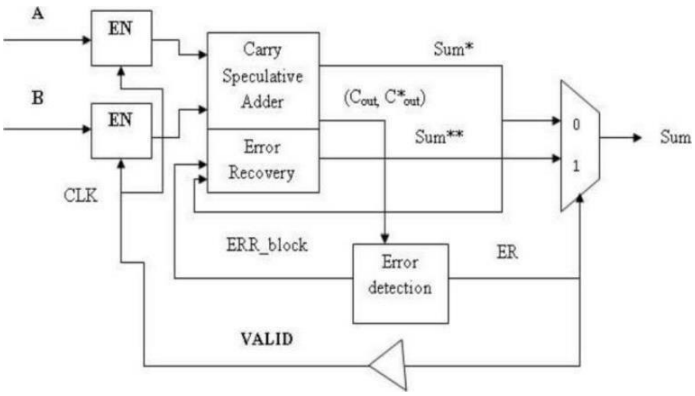
Figure2. Technological schematic of proposed BKA

BKA is one of the arithmetic adders. It occupies very little space. It has maximum depth. It is more efficient in terms of speed and power.

$$C^{i}_{out} = G^{i}_{x-1:0} + P^{i}_{x-1:0} C^{i-1}_{out}$$

B. SPECULATIVE ADDITION

Speculative addition is widely used in asynchronous design. The speculative addition involves two cycles. In the first cycle, the addition process is done and the end result is assumed as accurate sum. Meanwhile, a parallel carry propagation circuit checks whether the operation uses the carry long path known as the critical path. If it uses the longestpath the system requires the additional clock cycle to completethe addition process. If it didn't use the longest path, bypass logic is used to reduce the clock cycle required.



Speculative adders can overcome the area problem but it has high error rate. For this error tolerant variable latency adder is design upon the speculative adder. This variable latency adder consists of error recognition and correction circuit, which can overcome the high error rate and this design, helps the speculative adder to use in many applications such as image and signal processing.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Thus the design of speculation based BKA is simulated and synthesized. Here the different formats like XS-3, binary coded faster butthe possibility of occurrence of error is increased. Theproposed speculative adder can be able to complete the addition process quickly when compared to the existing technique speculative bit is calculated by the carry out bitof the window.

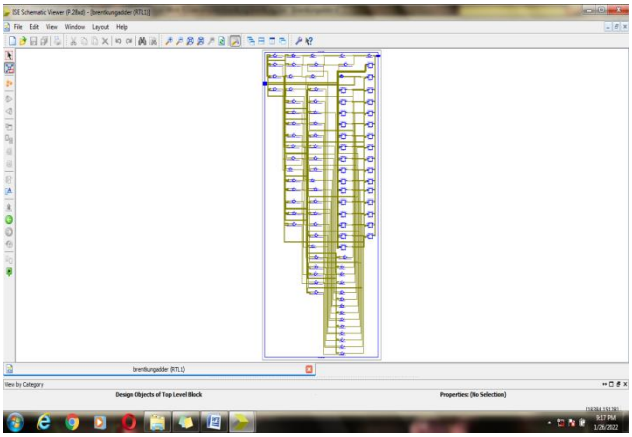


Figure4. RTL schematic view of proposed system

First cycle: addition is done without carry Second cycle: addition is done with Carry Speculative adder. It contains Brent-kung adder for performing both cycles. Enable and clock signals are used to enable inputs. Error detection unit is used to detect error in the inputs. Error recovery unit is there to perform ex-or operation to recover input from error. Two inputs are given to multiplexer. Based on selection line accurate output appears. Brent-kung adder is selected from block of adder. The reason behind using BKA, it provides less delay comparing other types of adders. There may be a tradeoff between delay and other parameter such as area, power, output accuracy etc., carry Select adder is widely used to improve performance of adders accuracy without increasing delay.

D. PERFORMANCE ANALYSIS

In this work, major VLSI performances of area, delay and power is obtained. Depends on the LUT, slices and IOB block utility, the area is calculated and net delay, path delay, static and dynamic power is calculated and compared with the previous work. There are two possible cases of errors. The major advantage is that the error detection unit can find which block adder prediction is wrong. By this advantage the work of the recovery circuit is simplified. The recovery circuit rectifies the affected block adder and corrects the output so that the output sum is accurate. This circuit is designed using varying latency design so that if an addition process is completed it send a valid signal to the input side to fetch another set of inputs to perform addition. A variable latency adder can combine the speculative logic with error recognition and correction forunsigned random inputs, called variable latency CSPA. The sum and carry generation are separated in CSPA and thus the carry signal and partial sum bit can be calculated faster. Carry predictor circuit of the block adder only to use input bits near the MSB to predict the carryout bit. The hardware cost of the prediction circuit is reduced and the CSPA has minimal error rate increase. The proposed error detection circuit indicates which block adder produced in incorrect carry-out bit, and the error recovery circuit only focuses on recovering the block adders with incorrect partial sum bits

IV. RESULTS AND DISCUSSION

Xilinx ISE (Integrated Synthesis Environment) is a software tool. It will be helpful for simulation as well as implementation. It can synthesis power distribution, delay, no of LUTs used, flooring plan and simulation results.

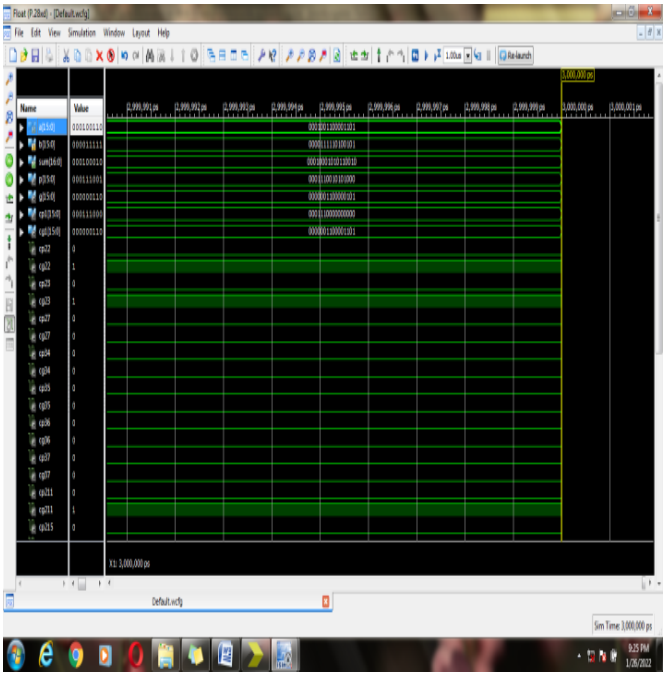


Figure5. Simulated result of proposed BKA

Table1. Device utilization summary report

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	32	1,920	2%
Number of occupied Slices	21	960	2%
Number of Slices containing only related logic	24	24	100%
Total Number of 4 input LUTs	43	1,920	2%
Number of bonded IOBs	49	66	74%

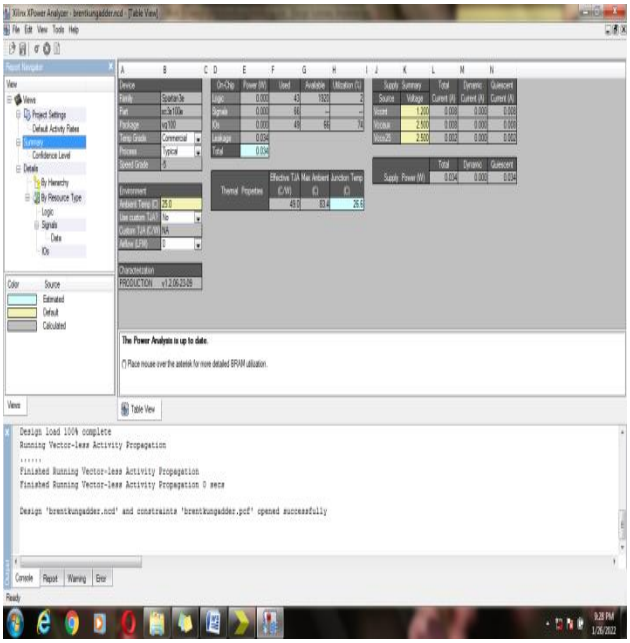


Figure6. XPower analyzer report

The CSA contains two ripple carry adders and one multiplexer. It performs addition with carry and without carry and generates accurate sum based on selection line of the multiplexer. A selected logic was suggested to speculate the carry input of each block based on some input operand bits of the current and next block.

Table2. Comparison results

Parameters	**BCSA without ERU using RCA**	**BCSA with ERU using RCA**	**BCSA with ERU using BKA**
Number of slices	24	23	21
Number of LUTs	33	33	32
Delay (ns)	13.97	13.372	12.022
Power(W)	0.172	0.172	0.034

Thus the simulation result of proposed work shows that number of LUTs, slices, delay and power is reduced than the existing works such as BCSA without ERU using RCA and BCSA with ERU using RCA.

V. CONCLUSION AND FUTURE SCOPE

In this paper, the proposed Brent Kung adder is improved with the energy efficient speculative adder for area efficient design. The carry speculation process is based on dividing an exact adder into some non-overlapped blocks operated in parallel states. Each block may be composed of any desired type of adders. In this we used carry select adder with Brent Kung adder logic. Based on the results, the different approximate operating modes are verified and VLSI circuit performance is achieved. Thus the design of carry speculation logic in parallel prefix adder of Brent Kung adder is designed and output performances are achieved than the previous literatures. In future, the work may be extended with the speculation logic based Brent Kung adder in VLSI filtering circuits and loss reduction circuit states.

VI. REFERENCES

[1]. H. Jiang, C. Liu, L. Liu, F. Lombardi and J. Han, "A review, classification and comparative evaluation of approximate arithmetic circuits," *ACM JETCAS*, vol. 13, no. 4, Article no. 60, 2017.

[2]. S. Mahlke. SAGE: self-tuning approximation for graphics engines. In Proc. *Micro*, 2013, pp.13-24.

[3]. H. Esmaeilzadeh, A. Sampson, L. Ceze, and D.Burger. "Neural Acceleration for General-Purpose Approximate Programs," In Proc. *of Micro*, pp.105-115, 2012.

[4]. B. K. Mohanty, S. K. Patel, "Area–delay–power efficient carry select adder", IEEE TCAS-II, vol. 61, no.6, pp. 418-422, Jun. 2014.

[5]. M. Bilal, S. Masud, and S. Athar, "FPGA Design for Statistics-Inspired Approximate Sum-of-Squared- Error Computation in Multimedia Applications," IEEE TCAS-II, vol. 59, no. 8, pp. 506-510, 2012.

[6]. M. Kamal, A. Ghasemazar, A. Afzali-Kusha, and M. Pedram, "Improving efficiency of extensible processors by using approximate custom instructions,"*DATE*, pp. 1449-1454, 2015.

[7]. W. Xu, S. S. Sapatnekar, and J. Hu. "A Simple Yet Efficient Accuracy Configurable Adder Design," In Proc. *ISLPED*, 2017.

[8]. R. Ye, T. Wang, F. Yuan, R. Kumar and Q. Xu, "On Reconfiguration- Oriented Approximate Adder Design and Its Application," In Proc. *ICCAD*, 2013, pp. 48-54.

[9]. M. Shafique, W. Ahmad, R. Hafiz and J. Henkel, "A low latency generic accuracy configurable adder," In Proc. *DAC*, 2015, pp. 1-6.

[10]. Swetha Bai and Vijay M, "Energy efficient Inexact speculative Adder using Carry look ahead adder and brent kung adder," International Journal of Innovative Research in Science, Engineering and Technology," 9(1):282-287, March 2020.

[11]. K Swetha Bai and S Vijay Murugan, "High speed inexact speculative adder using carry look ahead adder and brent kung adder," International Research Journal of Engineering and Technology, 7(3): 1006-1010, March 2020.

[12]. Mehnaz B, K Anil kumar, "Pipelined VLSI Architecture for In-Exact speculative adder using carry look ahead adder and brent kung adder," International Journal and Magazine of Engineering Technology, Management and Research, 6(1):32-42, 2019.

[13]. Jaiganesh, et al. (2017), "Speculative Han-Carlson adder for the improvement of speed of conventional carry skip adder," IJARIIE, 3(2), 2017.