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C E M 5 5 7 0

BUS CONTROLLED SIGNAL PROCESSOR

Preliminary, January 1987

Description

The CEM 5570 is an audio signal processing block controllable directly through a uP bus. Included on-chip are a wide range four-pole filter with selectable low-pass or band pass response, a variable gain amplifier for controlling the amount of filter resonance, and two variable gain amplifiers with separate inputs and outputs; also on-chip is a multiplying 12 bit DAC, five Sample & Holds, and associated latches and logic for controlling the four parameters -- filter frequency, filter resonance, gain 1, and gain 2.

Through use of a presample mode, and by driving the DAC reference input with a variable voltage source (such as an external DAC), the final parameter value may become the sum of two differently scaled 12 bit values (i.e. the sum of two products). Useful for coarse and fine adjustments or for software generation of controlling waveforms, this feature can save large amounts of real time computation by the controlling microprocessor. Flexibility is further enhanced with an exponential converter, which allows independently selectable linear or exponential control scales for any of the four parameters.

Since the filter is a continuous-time type, it avoids the problems of noise, distortion, and limited sweep range as well as the antialiasing and reconstruction requirements found with sampled data filters. The combination of 12 bit DAC resolution driving an exponential converter allows the entire 10 octave frequency range to be controlled in very fine equal frequency increments.

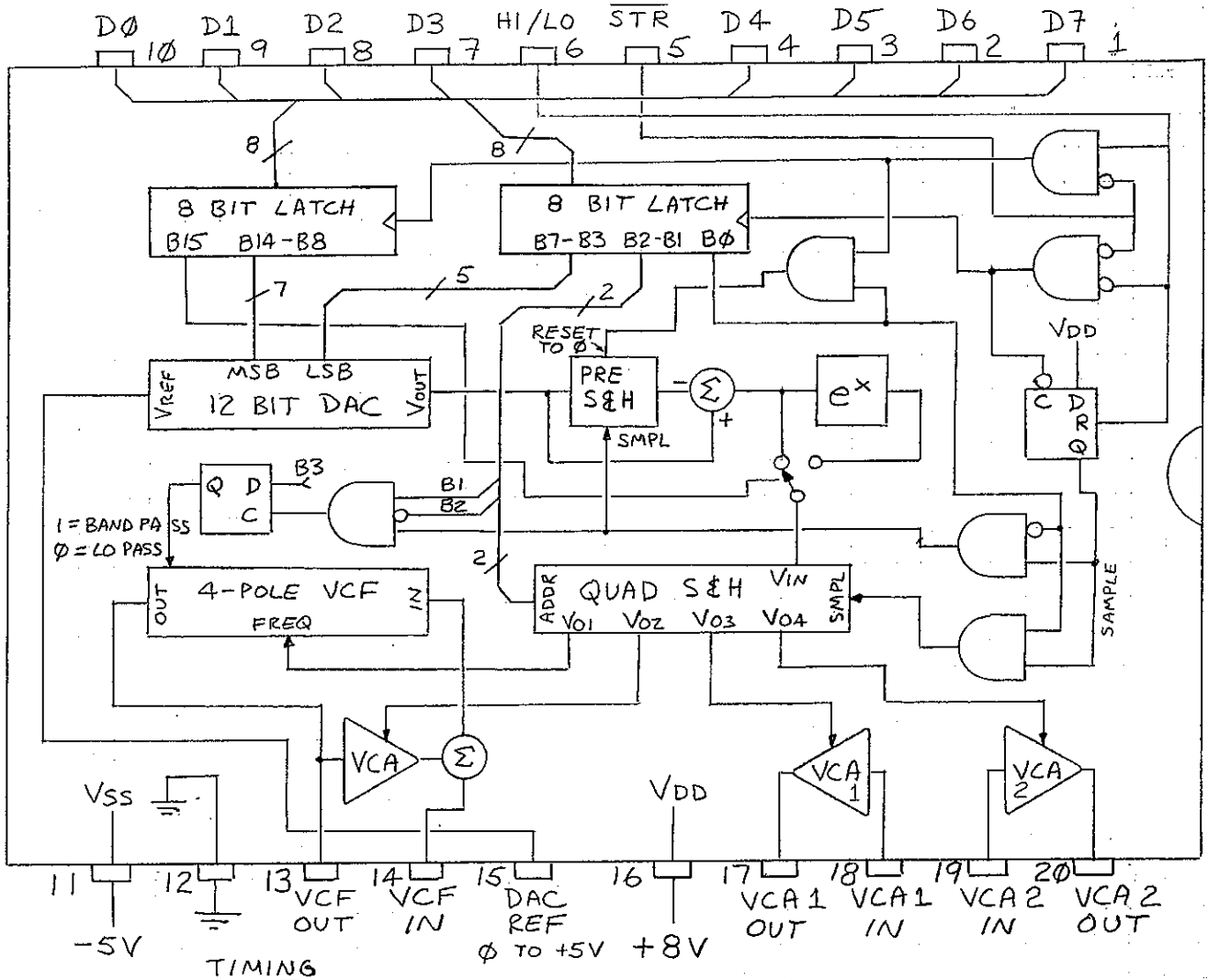
The resonance of the filter may be controlled from none at all (0dB of ripple) to self-sustained oscillation. The gain of the two amplifiers are variable from unity to in excess of -100dB; special circuitry guarantees 100dB of attenuation when 000H is programmed. Other features found in both the filter and amplifiers include large input signal handling capability, moderate input impedance, and voltage outputs capable of swinging 5 V.P.P. ($\pm$ 5V supply).

Requiring no external components, low in power drain, and directly interfaceable to a uP bus, the CEM 3370 is an ideal choice in digital systems requiring analog type audio signal processing.

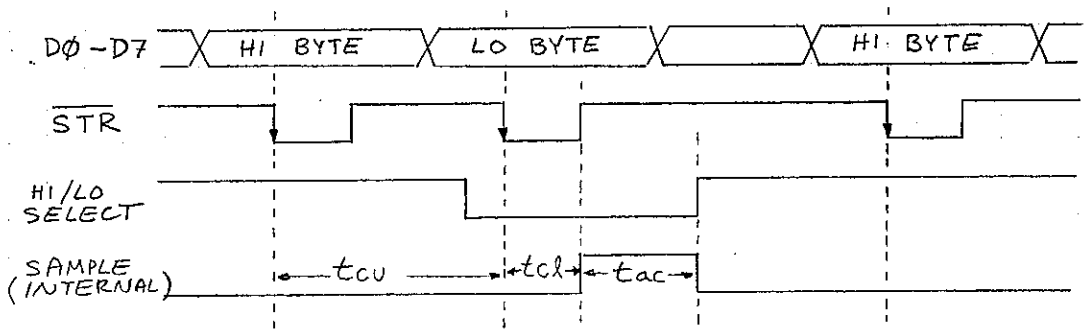
Features

- Signal processing functions controllable directly from the uP bus
- On-chip sum-of-2-products computation for all controlling parameters
- Continuous-time type of wide range 4 pole filter
- Selectable Low-pass or Band-pass filter response
- Large dynamic range variable gain amplifiers
- Selectable linear or exponential control scales for all parameters
- No external components
- 18 bit equivalent resolution with exponential scale, 12 bit resolution with linear scale, all with guaranteed monotonicity
- Tight absolute parameter tolerance: 5% on resonance and gain; 15% on filter frequency
- Excellent parameter scale linearity: Ø.5% on resonance and gain; 2% on filter frequency
- Low power drain: 12mA max

CEM 5570 BUS CONTROLLED SIGNAL PROCESSOR



TIMING



FOR HIGH BYTE: D0 - D6 = DAC 7 MSBs ; D7 = LINEAR/EXPO

FOR LOW BYTE: D0 = PRE-SAMPLE; D1-D2 = PARAMETER;
D3 - D7 = DAC 5 LSBs

11/1/86

VDD = +8V VSS = -5V TA = 20°C
VREF = +5v

Parameter	Min.	Typical	Max.	Units
LOGIC INTERFACE				
Logic Low Level	---	---	.8	V
Logic High Level	2.4	---	---	V
tzl, $\overline{STR}$ Transition	---	---	50	nS
tzh, H/L Transition	---	---	300	nS
tsd, Data Set-Up to $\overline{STR}$ ↓	50	---	---	nS
thd, Data Hold from $\overline{STR}$ ↓	500	---	---	nS
twh, STR Pulse Width (H/L high)	800	---	---	nS
tcl, STR Pulse Width (H/L low) [1]	10	---	---	uS
tcu, $\overline{STR}$ ↓ (H/L High) to $\overline{STR}$ ↓ (H/L Low)	50	---	---	uS
tac, $\overline{STR}$ ↓ to H/L ↓	3	---	---	uS
tss, $\overline{STR}$ ↓ to H/L ↑	500	---	---	nS
tsh, H/L to $\overline{STR}$ ↑	50	---	---	nS
DAC & C.V. PROCESSING				
Resolution	---	12	---	bits
Full Scale Linearity	---	0.1	---	%
Monotonicity	12	---	---	bits
Offset [2]	---	---	10	LSBs
Full Scale Settling Time to 1 LSB for Pre Sampling	---	15	---	uS
Full Scale Settling time to 1 LSB for Final Sampling [3]				
Linear Mode	---	65	---	uS
Exponential Mode [4]	---	160	---	uS
Sample & Hold Access Time	---	2	---	uS
Sample & Hold Refresh Time for 1 LSB Droop	2	10	---	mS
Sample to Hold Step	---	---	5	LSBs
Reference Input Resistance	---	6	---	Kohm
FILTER				
Cut-off Frequency Range				
Linear Mode [5]	---	8	---	octaves
Exponential Mode [6]	---	14	---	octaves

Cut-off Frequency[7] for Data=4095				
Linear Mode	---	25	---	KHz
Exponential Mode	---	16	---	KHz
Linear Scale Factor	---	6	---	Hz/bit
Exponential Scale Factor	---	340	---	LSBs/ octave
Tempco of Cut-Off Frequency				
Linear Mode	---		---	%/°C
Exponential Mode	---		---	%/°C
Resonance Data Input for self oscillation - Linear Mode Only	---	3700	---	
Oscillation Output Amplitude	---	2	---	V.P.P.
Distortion for 5 V.P.P. Inputs	---	---	3	%
Passband Gain	---	1.0	---	
Output Noise[8]	---	0.5	---	m.V.R.M.S.
DC Output Shift 10Hz - 10KHz	---	±50	---	mV
Signal Input Resistance	---	50	---	Kohm
Output Swing	---	---	6	V.P.P
Output Load Capability for 5V.P.P. output	20	---	---	Kohm
VCAs				
Gain for Data = 4095				
Linear Mode	---	.9	---	
Exponential Mode	---	.6	---	
Attenuation for Data = 0[9]	85	---	---	dB
Linear Scale Factor	---	0.022	---	%/bit
Exponential Scale Factor	---	0.018	---	dB/bit
Tempco of Gain				
Linear Mode	---		---	%/°C
Exponential Mode	---		---	%/°C
Distortion for 5V.P.P Input	---	---	3	%
Output Noise[8]	---	0.5	---	mV.R.M.S
DC Output Shift, Min to Max Gain	---	±50	---	mV
Signal Input Resistance	---	68	---	Kohm
Output Swing	6	---	---	V.P.P.
Output Load Capability for 5V.P.P. Output	20	---	---	Kohm
GENERAL				
Supply Voltage Range[10]				
Positive	4.5	---	10	V
Negative	-10	---	-4.5	V
Supply Current	---	8	---	mA
DAC Reference Voltage[11]	---	---	5.5	V

NOTES:
1. For presample mode. See application hints for other required times.
2. Includes offset from PRE Sample & Hold, Summer, and other processing circuitry.
3. Includes DAC output processing circuitry.
4. From low to high; high to low is 30% shorter.
5. Presample not used.
6. Presample used to generate negative voltage.
7. -1dB point and oscillation frequency.
8. 16-16KHz bandwidth. Data = 4095. 15dB less at Data = 0.
9. Re: maximum output.
10. Max supply across chip is 16V.
11. Must always be $\geq$ 0 and < VDD. See application hints.

TABLE A: Bit Assignment of Data Input to CEM 5570

Data High Byte

D7: 0=Linear Scale; 1=Exponential Scale
D6: DAC Bit 11 MSB
D5: DAC Bit 10
D4: DAC Bit 9
D3: DAC Bit 8
D2: DAC Bit 7
D1: Dac Bit 6
D0: DAC Bit 5

Data Low Byte

D7: DAC Bit 4
D6: DAC Bit 3
D5: DAC Bit 2
D4: DAC Bit 1
D3: DAC Bit 0 LSB
For resonance presample, 0=VCF low-pass; 1=VCF Band-pass

D2: {parameter}	0 = VCF	0 = VCF	1 = VCA1	1 = VCA2
D1: {select }	0 = Frequency	1 = Resonance	0 = Gain	1 = Gain

D0: 0=Present DAC value will be presampled only
1=Present DAC value minus any presampled value will be sampled into selected Final S&H

Power Supplies

As long as the voltage between VDD (pin 16) and VSS (pin 11) is not allowed to exceed 16V, then the positive supply, VDD, may range from 4.5V to 10V, while the negative supply, VSS, may be between -4.5V and -10V. The other restriction is the maximum DAC reference voltage input allowed for proper DAC operation, calculated by the following:

$$VREF\ MAX = .8VDD - .2VSS - .4$$

Thus, with ±5V supplies for example, the largest DAC reference input is +2.5V. For a +5V reference, supplies of +8V, -5V or +9V, -6V are recommended. Although the reference voltage can be made negative by 1-2 volts, there is no reason to do so, and it is recommended that it be maintained Ø and positive.

The voltage selected for the DAC reference determines the range of the VCF and VCA parameters: The values given in the specifications are for a reference of 5V; for voltages less than this, the maximum VCF frequency and VCA gains as well as the scale factors must be scaled down proportionally.

The negative supply affects the amount of sink current drive possible from the VCF and VCA outputs according to the following:

$$Io\ (mA) = .1\ (Vss-Vo+1)^2 + Vo/25$$

Thus, for an output of Vo = -2.5V, the maximum current sink is 125uA (minimum load of 20K) at Vss = -5V, and 525uA (minimum load of 4.7K) at Vss = -6V. Since up to 2mA can be sourced by the outputs, the sink capability may be increased with an external pull down resistor to preferably a supply more negative than Vss. For example, a 10K resistor to -12V will provide 1mA source and sink capability (2.5K minimum load).

The logic input threshold levels are unaffected by either supply.

Basic Operation and Logic Interface

Interface to the VCF and VCAs consist of two 8 bit latches, a 12 bit DAC, Pre Sample & Hold, DAC output voltage processor, four addressable Sample & Holds, and control logic. The DAC voltage processor includes the summer, exponential converter, and other processing circuitry.

The logic inputs consist of 8 data inputs, a $\overline{STR}$ signal which clocks the data on the negative edge into the high byte latch when HI/LO is high, and into the low byte latch when HI/LO is low. As shown in Table A, the high byte contains the "scale" bit (linear or exponential) and the DAC 7 most significant bits. The low byte contains the DAC 5 least significant bits, 2 parameter

select bits, and Pre S&H or final S&H select bit. For proper operation, both bytes are required with the low byte always following the high byte to produce a completed voltage sample.

The DAC output voltage is sampled into the Pre S&H or selected final S&H only upon the low byte $\overline{STR}$ signal (H/L low) returning high and then held in the S&H when the HI/LO signal also returns high. (Please refer to the timing diagram in Figure 1). Thus, the time between the high byte $\overline{STR}$ negative edge and low byte $\overline{STR}$ positive edge is required for the DAC and processing circuitry to settle, while the time between low byte $\overline{STR}$ positive edge and H/L positive edge is required for the selected S&H to acquire the new voltage level.

When the Pre S&H is selected (low byte BØ = Ø), the DAC output resulting from the 2 byte sequence is stored only in this S&H and the four final S&Hs are left unaffected (B1 and B2 affects only the filter response). Then, the DAC output resulting from the next 2 byte sequence combines with the negative of the Pre S&H value (applications of this will be described later) and, if BØ of the low byte is a 1, the combined value is sampled into the final S&H selected by B1 and B2 (a presampling 2 byte sequence following a presampling sequence will not alter the first presampled value). Finally, whenever any selected final S&H returns to the hold mode after sampling, the value in the PRE S&H is reset to Ø.

Thus, using the PRE S&H requires a sequence of 4 bytes for proper operation--high byte followed by low byte of the presample value followed by high byte and then low byte of the final value. Note that the presample mode can be used selectively for any, none, or all parameters: A 2 byte sequence with low byte BØ=1 following a 2 byte sequence with low byte BØ=1 will encounter the Pre S&H reset to Ø and therefore not affecting the final parameter value.

The filter consists of four 1-pole sections controlled by the same value from S&H Ø (B1=Ø B2=Ø); the first section has selectable low pass or high pass response, while the last 3 sections are fixed at low pass only. Thus, the overall response is selectable either as low pass with 24dB/octave cut-off slope, or a bandpass with 6dB/octave rising slope and 18dB/octave falling slope. In addition, a feedback transconductor controlled by S&H 1 (B1=1 B2=Ø) allows a variable amount of peaking (resonance) to be added at the cut-off frequency; beyond a certain value, the filter will break into self-sustained oscillation at the cut-off frequency (approximately -1dB point).

The filter response is selected during the presample mode where low byte BØ=Ø and B1=1, B2=Ø; during the same time that the PRE S&H is being sampled, a low byte B3=Ø will cause the low pass response to be selected while B3=1 will cause the bandpass to be selected. Since B3 (the least significant DAC bit) also affects the value stored in the PRE S&H, it is recommended that: a) all other DAC bits be set to Ø during response selection, and b) that the following 2 byte sequence update the resonance S&H so that

the previous presample value only affects the resonance LSB (not noticeable). Note this 2 byte presample sequence only needs to be done once to change the filter response.

The gain of VCA1 (pin 18 to pin 17) is controlled by S&H 2 (B1=Ø B2=1) while the gain of VCA2 (pin 19 to pin 2Ø) is controlled by S&H 3 (B1=1 B2=1). Because of the DAC processing offsets, with linear scale selected the gain can become Ø at a programmed value as high as 1Ø or can be as high as -5ØdB at a programmed value of 1. To prevent possible high leakage due to offsets, switches and logic has been added to squelch the VCA gains to below -85dB when a programmed value of Ø is detected.

Both filter and VCAs accept a nominal input level of ±2.5V Peak (5V.P.P.) for moderate distortion. Lower distortion may be achieved by lowering the input level, but at the expense of reduced signal-to-noise ratio. Nominal input impedance to these analog blocks is 5ØK, and maximum gains around unity. The outputs of the two VCAs as well as the filters are low impedance voltage outputs with moderate drive capability. Hence, op amp current to voltage converters are not required, and system configurations are implemented by directly connecting outputs to inputs without the need of any external components.

Selection of Interface Timing & Hardware

Selection of the proper timing intervals between $\overline{STR}$ and HI/LO transitions (proper timing sequence has been discussed above) requires consideration of settling times through the control voltage chain. Although the DAC can settle to less than 1 LSB in less than 1ØuS, the circuitry after the Pre S&H and summer is relatively slow. With linear scale selected, this circuitry responds with an RC time constant of around 8uS; a full transition of the 5 least significant bits hence requires 3ØuS to settle to 1 LSB, while a full scale settling of all bits to 1 LSB requires 65uS. With the exponential scale selected, the overall response RC time constant is 2ØuS (15uS from 2Ø48 to 4Ø96); this results in 5 LSB settling and full scale settling time of 75uS and 16ØuS respectively.

To maintain parameter accuracy at 1 LSB for worst case data changes, the interval between negative edge of high byte $\overline{STR}$ and positive edge of low byte $\overline{STR}$ should be at least the full scale settling time (65uS linear, 16ØuS exponential), and the low byte $\overline{STR}$ pulse width should be at least the settling time for the 5 LS bits (3ØuS linear, 75uS exponential). If more error can be tolerated, or if parameter changes will always be small (such as during ramping) and the previous parameter is stationary, then these required time intervals can be shortened.

Note that these long times are only required for strobing into the final S&Hs; for presampling, $\overline{STR}$ to $\overline{STR}$ interval only needs to be 15uS long and low byte $\overline{STR}$ pulse width may be as short as 1ØuS to achieve 1 LSB accuracy.

In most applications, interfacing to a microprocessor system may be accomplished simply by generating H/L from a single bit of an I/O port and deriving the $\overline{STR}$ signal from the processor generated I/O write or memory write pulse. To meet the settling time requirements, the $\overline{STR}$ pulse must be made longer than the usual write pulse: if the data is valid at the falling edge of the write pulse, a pulse stretcher such as shown in figure 2 may be used to generate $\overline{STR}$; if the data is valid at the rising edge (such as with multiplexed data and address bus), then a positive edge triggered one-shot such as shown in figure 3 may be used.

Of course, this $\overline{STR}$ signal must be enabled only when writing data to the 5570; a convenient way to do this in a system with multiple 5570s is with a HC138 as also shown in figure 3, where the H/L signal is common to all 5570s in the system. In such an interface, each 2 (or 4) byte sequence needed to update a parameter must be completed before the next byte sequence is begun for updating the next parameter. Allowing just one parameter to have an exponential scale requires that the $\overline{STR}$ signal be 80uS wide (for 1 LSB accuracy under worst case data changes); hence a 2 byte sequence will require a minimum of around 170uS and updating 32 parameters will take over 5mS. Assuming the microprocessor is tending to other tasks in between data writes to the 5570s, this time is acceptable in many applications.

When shorter update times are necessary, a different interface approach may be used. Independent $\overline{STR}$ signals and HI/LO signals for each 5570 are generated from separate I/O bits (e.g. 16 I/O bits for 8 5570s). Not only does this allow the width of each $\overline{STR}$ signal to be controlled by software and hence lengthened or shortened according to the settling requirements of the particular parameter being updated, but more importantly it allows overlapping of the $\overline{STR}$ and H/L signals for further improved efficiency. The timing for such a system is shown in figure 4, where update time for 32 parameters can be accomplished in less than 1mS while still allowing 168uS for DAC voltage settling. This technique also requires an 8 bit wide data latch (one for all 5570s) to which the appropriate data bytes are written just prior to writing to the $\overline{STR}$ and H/L I/O ports.

Applications of Pre Sample and Holds

The purpose of the presampling feature of the 5570 is essentially to generate the same effect as having 2 Sample & Holds controlling each parameter. The presampling in conjunction with the fact that the DAC reference is external and variable (i.e. the DAC is multiplying) allows each parameter to be a combination of two differently scaled 12 bit values. This function is accomplished by applying a voltage to the reference input (pin 15) during presampling which is different than the voltage applied during final sampling. The reference voltage could be changed with an external DAC (for many bits of resolution) or

simply with a CMOS switch (for selection of only 2 possible values); any change in the DAC reference should be made after the HI/LO signal returns from low to high, but prior to the $\overline{STR}$ signal falling low.

Thus, one application of the Pre S&H is to allow both "coarse" and "fine" control over any parameter, where a normal 5V reference is used for the regular sampling while some smaller value (e.g. 5/16V) is used for the presampling. In this way, the presample value allows fine adjustment of the control voltage between DAC LSBs of the final value. (Although this technique effectively increases the resolution of the final parameter, it does not provide the monotonicity of a higher order--16 bit for example--DAC.)

A use for such coarse and fine adjustment is the software correction of both the initial frequency and scale factor of the VCF, for example, where the final data is always the same for any given frequency for all 5570s in a system, while the presample data is used to correct the normal unit to unit variations. Another use for the fine control is to adjust out any gain control offset in the VCAs, so that the gain with a linear scale corresponding to a data input of 1 is that expected (i.e. 1/4096 = -72dB).

This last example demonstrates one reason for the polarity inversion of the presample before being summed with the final sample: The negative fine control of the Pre S&H allows positive offset to be nulled to zero which otherwise would not be possible. Another advantage of the negative output of the Pre S&H is that it allows the filter frequency to be driven even lower than the value at a data input of 0 (approximately 4HZ in the exponential mode). In such a case, the reference voltage is always kept the same, but the data input is applied to presample instead of the final sample, and the final sample is set to 0.

An important application of the sum-of-two-products capability of the 5570 is to generate for any parameter a sum of a static value and a software generated controlling waveform with variable amplitude (such as a dynamically controlled envelope in music applications). For such an application, the reference voltage is controlled by an external DAC (e.g. 8 bits) for varying waveform amplitude; the static value is set by the main S&H while the variable waveform is generated through the Pre S&H. The negative polarity of the outputted presample voltage must be taken into consideration as follows: Let the waveform data, called Nwav swing between 0 and 4095, where higher numbers produce an increasing final effect (in frequency, gain, or resonance). Then, the external reference DAC is set for the desired waveform amplitude, and the data (number) loaded into the Pre S&H becomes:

4095 - Nwav

Next, the reference voltage is set to its maximum (5V) and the data (number) loaded into the main S&H becomes:

$$Nstat + (4095 - No) \times (Vpreref / Vmainref)$$

where Nstat is the desired final static value for the parameter, where No is the waveform starting value before amplitude information (i.e. No = 0 for positive going waveform, = 4095 for negative only going waveform, or = 2047 for symetrical plus and minus going waveform), Vpreref is the reference voltage for presampling (amplitude information), and Vmainref is the reference voltage for main sampling (normally a constant value of 5V). Note that only one software multiplication is needed for a change in amplitude value, except for negative only going waveforms (No = 4095) which require no multiplication. As can be seen from this example, the Pre S&H contained in the 5570 eliminates the need for multiplication of every single data point in the waveform for controlling its overall amplitude, thus saving considerable software number crunching.

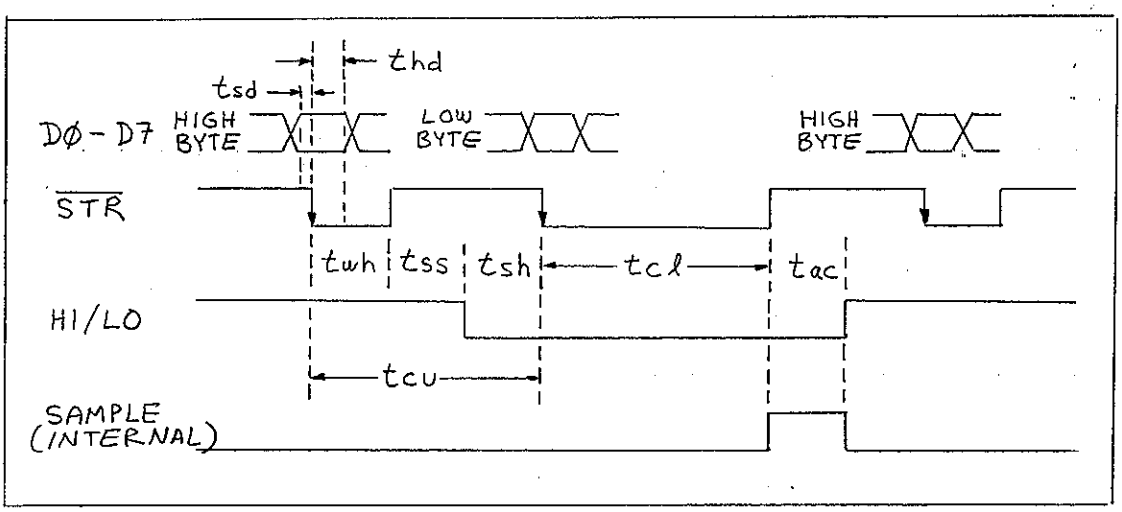


FIGURE 1: CEM5570 BASIC TIMING

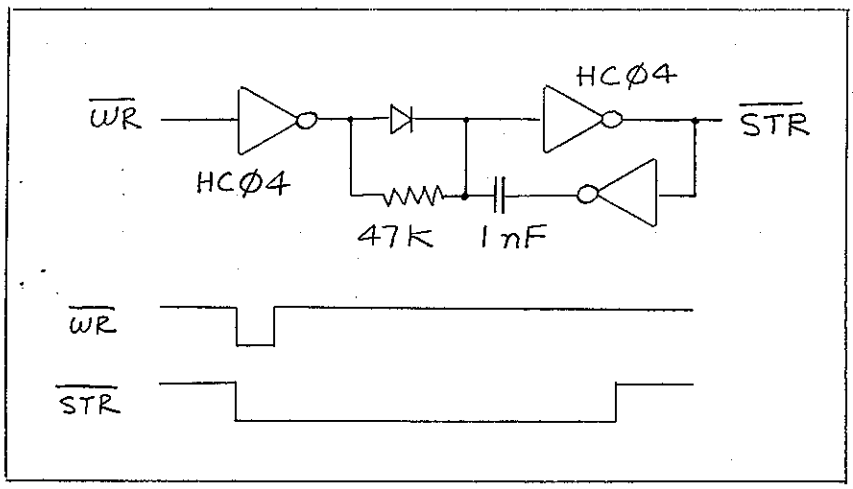


FIGURE 2: PULSE STRETCHER

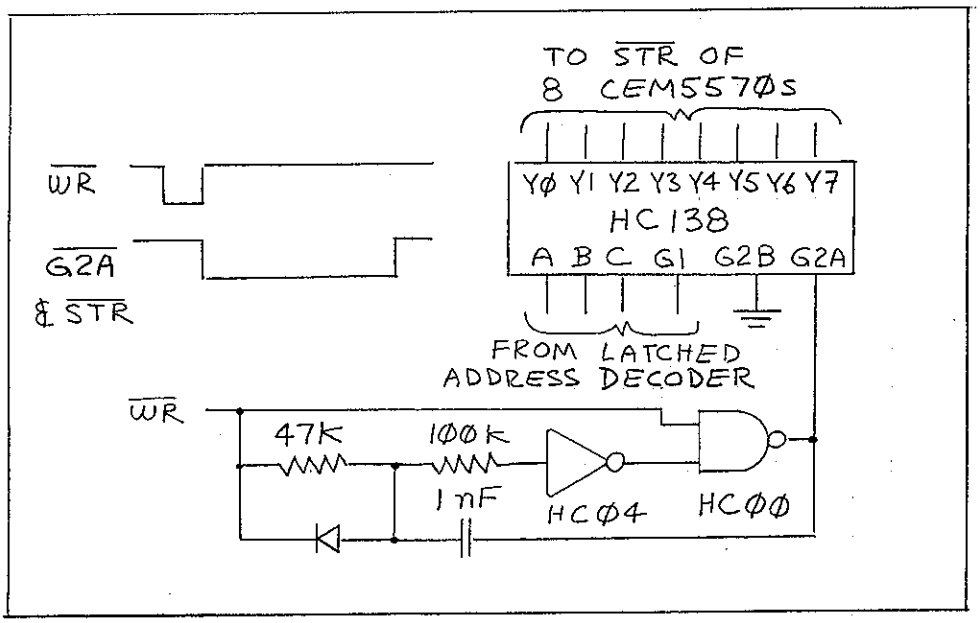


FIGURE 3: INTERFACE TO MULTIPLE CEM5570s (METHOD 1)

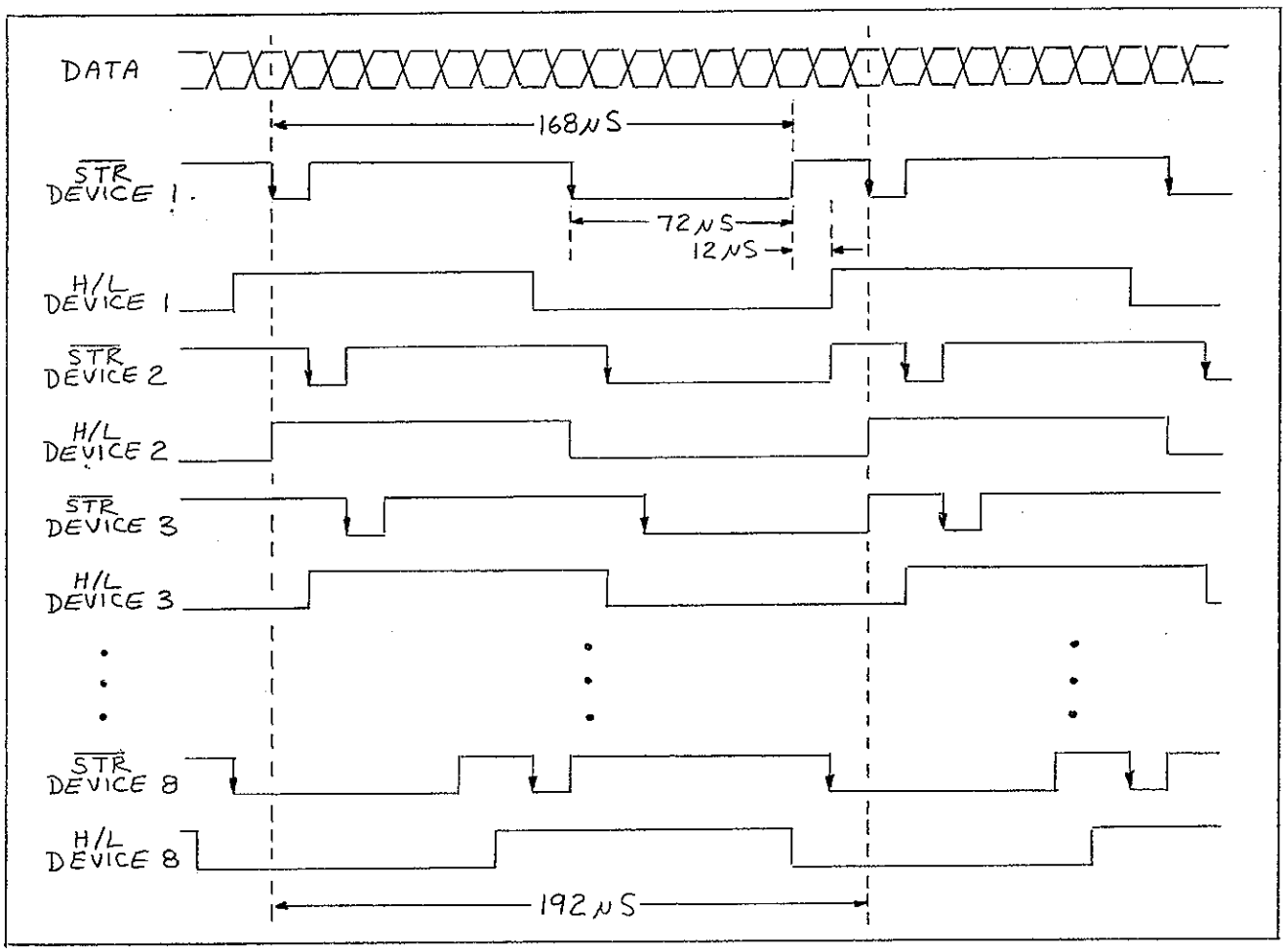


FIGURE 4: INTERFACE TIMING TO MULTIPLE CEM5570s (METHOD 2)