An Efficient Flash Memory Design Using FinFET Technology

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Abstract— The main requirement of consumers in electronic gadgets is more memory and less power consumption. Depending on these requirements, manufacturer designed all semiconductor memories with shrinking the size of device by scaling the transistor. Generally we have different semiconductor memories. Among those we prefer more on flash memories, due the simple to manufacturing and high speed of storing capability. NAND array and NOR array are basic type of flash memories which are used in all types of electronic gadgets. By scaling the floating gate MOS transistor leads to occurs Short channel effects. Infloating gate transistors, we required more voltage to store bit of information. For these parameters we designed FinFET based flash memories which had less leakage power and low power consumption devices. We verified FinFET based flash memories in PTM 45nm Technology node. Final we compared the power consumption of two technologies.

Keywords— *Short channel effects, FinFET, Scaling, Flash Memories, CMOS.*

I. INTRODUCTION

FinFET is consider as mosfet which can built on substrate where barrier is placed on two, three and four sides of channel and form double gate structure. Then they give name as FinFet based on source/drain region formed on silicon surface external. A flash memory can form on Non-Volatile Read Write Memory which is used for rewrite memory chip and unlike as RAM chip, there is no need off power supply required for the memory.

It has a capability to erase and reprogrammed by using electrically. Flash memory is first expanded by TOSHIBA in 1980's. Flash memory is very long-lasting and can stand on both extreme pressure and extreme temperatures. It is mainly used in memory cards, USB flash drives etc. This paper will focus on the fundamental elements of non-volatile memories. Theyare Differenttypes of Flash memory cells has been there but today two of them are standard, they are the neither common ground NOR Flash and the NAND Flash. The connection between memory cell and memory array performance limits are introduced in NAND and NOR array architectures.

II. SEMI CONDUCTOR FLASH MEMORIES:

Flash memory has many features. It is a lot less expensive than EEPROM and does not require batteries for solid-state storage such as static RAM (SRAM). It is non-volatile, has a very fast access time and has a higher resistance to kinetic shock compared to a hard disc drive. Flash memory is extremely durable and can withstand intense pressure or extreme temperatures. It can be used for a wide array of applications such as digital cameras, mobile phones, laptop computers, PDAs (personal digital assistants), digital audio players and solid-state drives (SSDs). Basic Semiconductor memories show in below figure.

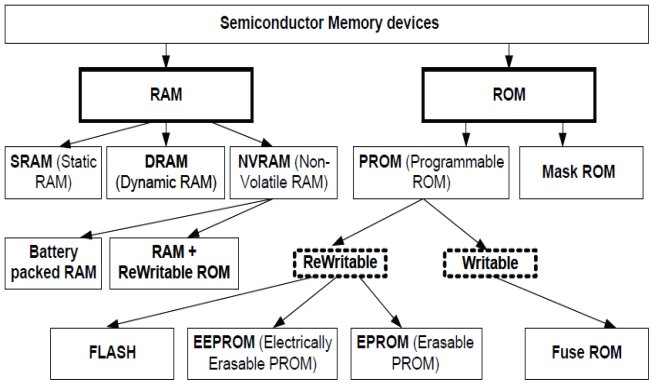

Fig.1 Basic Electronic Semiconductor memory devices.

A. NAND Flash Memory:

NAND Flash technology is considered as core of code and data can storage in mobile and embedded applications. It was succeed by TOSHIBA in 1989 as memory array architecture. It has both logical operator based on logical AND and logical NOR. In a NAND flash architecture a drifting gate cell placed on NAND string ends connected with a select line and a bit line.It is more favored Solid State Drives (SSD) which can restore on Hard Disk Drives (HDD). To this extent, many attempts was spent on both research and development of a suitable platform which can be address at the same time reduced fabrication costs, high storage density authorize by the multi-bits per cell. The NAND Flash array isassembling into a series of blocks, which are consideringsmallest erasable operations in NAND Flash device. An important goal of NAND flash array is to reduce in cost per bit and increase maximum chip capacity based on flash static read-only memory (ROM) or random access memory (RAM). The technology is protecting from shock resistant and can stand on both high and low

temperatures, as well as flash flood in water, so it achieve better than hard disks in mobile devices.

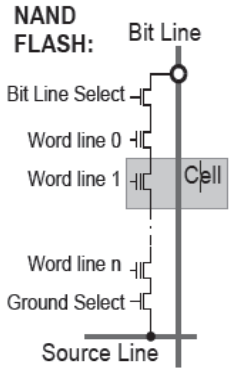

Fig.2 NAND Flash Memory cell structure [1]

B. NOR Flash Memory:

NOR flash array is also developed by TOSHIBA but first introduced by INTEL in 1988. A NOR flash can be read a when compared to NAND flash a little bit faster. It is more comfort to store code in embedded systems. A perfect example for an electrically erasable and programmable Read Only Memory. Each NOR flash cell has large memory can compete with magnetic storage devices, such as hard disks. NAND flash has begun in market in devices to which large files are many times uploaded and replaced. MP3 players, digital cameras and USB flash drives use NAND technology.

NAND flash can only support only small number of write cycles per block. It transfer rapid read access, but it's slow when compared with NAND flash cell. It supports only byte random access and faster access in order to complete memory. NOR is a logical operator consists of logical OR and logical NOT and returns a true value both the operands are false. A NOR has to write larger and bigger blocks of data at a time. In a classical NOR array each cell has a contact with the bit line which increases the effective cell size.

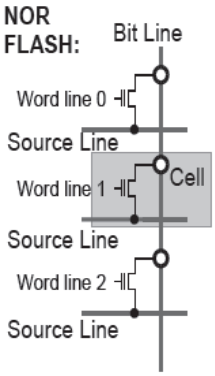

Fig.3 NOR Flash Memory cell structure [1]

III. MOS FLOATING GATE FLASH MEMORIES:

For flash memories we are using floating gate MOS transistors. The previous technologies so far in use are planar CMOS technologies. The CMOS technology was invented by Frank wanlass. A CMOS is a combination of a p-type and an n-type MOSFET. It is used in microprocessors, integrated circuits, sensors, microcontrollers, RAM. The demand for faster devices can be achieved by scaling the CMOS from millimeters to nanometers. Let's compare the CMOS technologies with FinFET technologies.

A. 2 Bit NAND Array:

In two bit NAND array structure we have three transistors with Bit Line, Word Line and Source Line. As we have Word Line is enable only then Bit Line information stored in the location through the reference of source line.

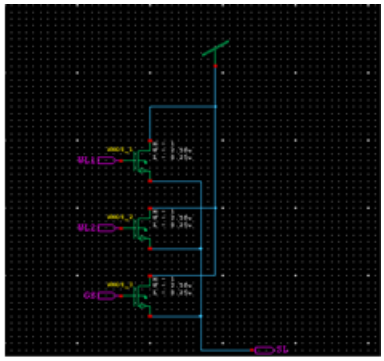

Fig. 4 Schematic of 2Bit NAND Array

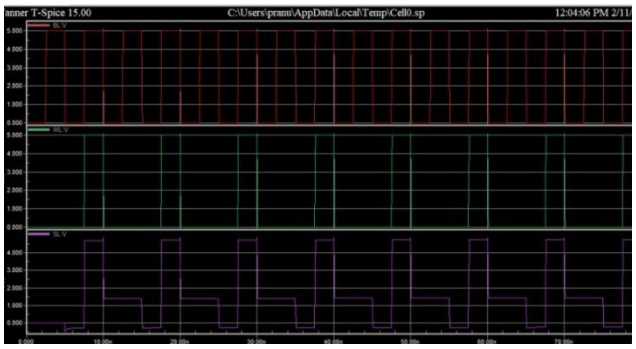

Fig 5 Simulation Result of 2BIT NAND Array

B. 2 Bit NOR Array:

In two bit NOR array structure we have two transistors with Bit Line, Word Line and Source Line. As we have Word Line is enable only then Bit Line information stored in the location through the reference of source line. As like the Nor gate simulation.

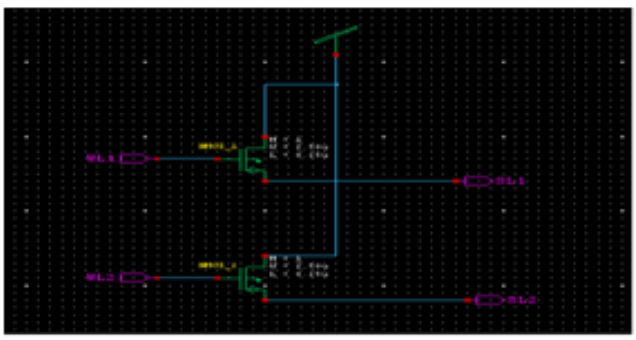

Fig. 6 Schematic of 2Bit NOR Array

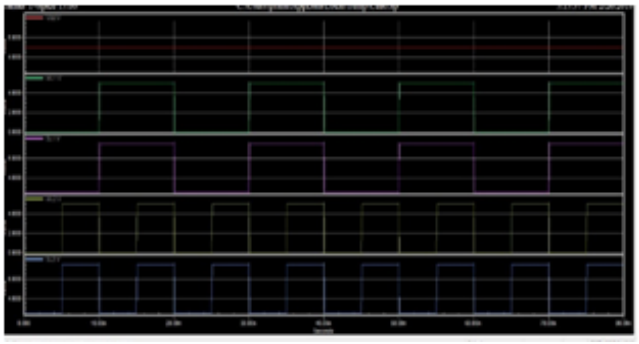

Fig 7 Simulation Result of 2BIT NOR Array

A 4 Bit NAND Array:

In four bit NAND array structure we have five transistors with Bit Line, Word Line and Source Line. As we have Word Line is enable only then Bit Line information stored in the location through the reference of source line. As we want to store more number of bits then we want to follow Fig 10 Schematic of 4Bit NOR Arraythe structure with more number of floating gate transistors.

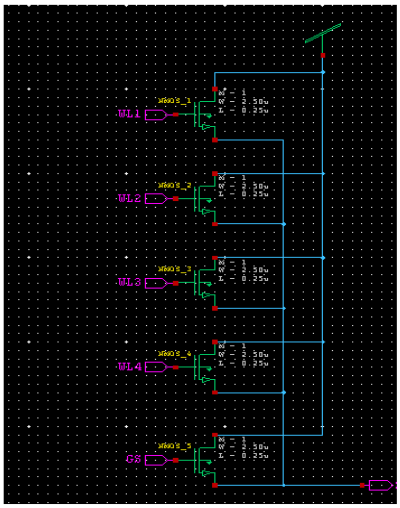

Fig. 8 Schematic of 4Bit NAND Array

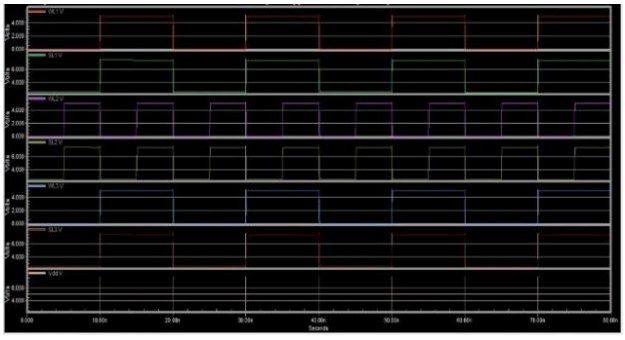

Fig 9 Simulation Result of 4BIT NAND Array

B. 4Bit NOR Array

In four bit NOR array structure we have four transistors with Bit Line, Word Line and Source Line. As we have Word Line is enable only then Bit Line information stored in the location through the reference of source line. As we want to store more number of bits then we want to follow the structure with more number of floating gate transistors.

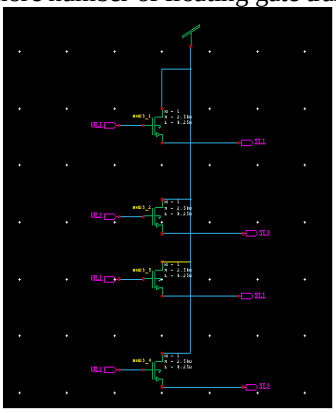

Fig. 10 Schematic of 4Bit NOR Array

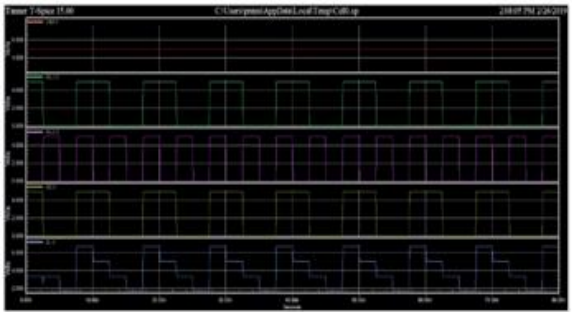

Fig 11 Simulation Result of 4BIT NOR Array.

IV. FinFET FLOATING GATE FLASH MEMORIES

As we already discussed about FinFET technology. As we shrink or scale down the transistor channel or source to drain distance then we have some major drawbacks named as Short Channel Effects. The basic short channel effects are Drain Induced Barrier Lowering (DIBL), Punch Through, Hot Electron Effect, and Velocity Saturation. For that reason we are Assigning additional gate to control the sub threshold leakage current. As we use this technology still we have very less source and gain channel distance. So we verified FinFET based Flash memories give you less power consumption as well as less leakage power. We considered PTM based 45nm MOS transistor and 45nm FinFET model. And we observed the both parameters.

Table1 Comparison of two technologies Power Consumption.

Performance parameter	CMOS Technology		FinFET Technology		% REDUCTION
	NAND	NOR	NAND	NOR	
Avg. power Consumption (2-Bit)	220µW	424µW	58.24nW	58.6nW	110%
Avg. power Consumption (4-Bit)	920.3 µW	916µW	78.231nW	67.52nW	90%

V. CONCLUSION

As we discussed about CMOS based NAND and NOR Flash memories. By considering CMOS floating gate Flash memories we want to apply high voltage to have conduction between floating gate and channel. This leads to have high power consumption while we have stored the bit. Hence we designed FinFET based Flash memory which consumes very less power as well as less sub-threshold leakage current. We concluded FinFET based NAND and NOR array which have efficient power consumption and less leakage current.

VI. REFERENCES

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