4-Mbit (128K x 36) Pipelined SYNC SRAM

Part Number: DPA71350G02A

\ The DPA71350G02A is a 3.3V, 128K x 36 synchronous-pipelined Burst SRAM designed specifically to support unlimited true back-to-back Read/Write operations without the insertion of wait states. The DPA71350G02A is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive Read/Write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of the SRAM, especially in systems that require frequent write/read transitions.

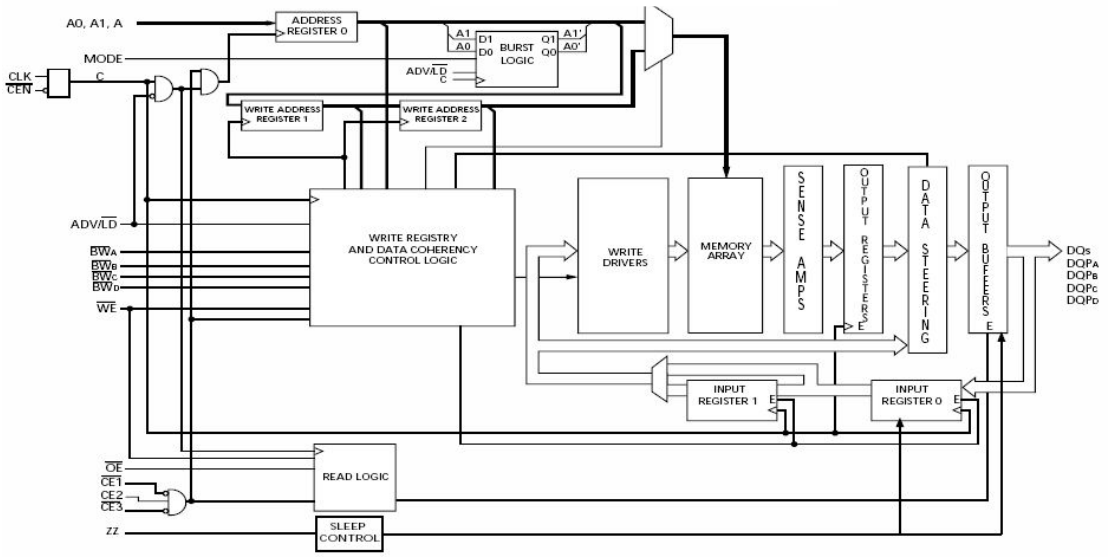
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ($\overline{CEN}$) signal which, when deasserted, suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 2.6 ns (250-MHz device).

Write operations are controlled by the four byte write select ($\overline{BW}_{[A:D]}$) and a write enable ($\overline{WE}$) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provides for easy bank selection and output tri-state control. In order to avoid bus contention, the output drives are synchronously tri-stated

- **-55˚ to +125˚C operating temperature**
- **Hermetically sealed ceramic packaging**
- **Internally self-timed output buffer control to eliminate the need to use $\overline{OE}$**
- **Byte Write capability**
- **218K x 36 common I/O architecture**
- **3.3V power supply**
- **2.5V or 3.3V I/O power supply**
- **Fast clock-to-output times**
  - **2.6 ns (for 250-MHz device)**
- **Clock Enable ($\overline{CEN}$) pin to suspend operation**
- **Synchronous self-timed writes**
- **Asynchronous output enable ($\overline{OE}$)**
- **Burst Capability-linear or interleaved burst order**
- **"ZZ" Sleep mode option**
- **This product uses Cypress CY7C1350G die and is tested to meet military and space operational environment requirements.**

Logic Block Diagram



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