Design and Analysis Modified Multilevel Converter Renewable Energy Applications

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ABSTRACT- Now a day's solar fed cascaded multilevel inverter is used to reduce the number of semiconductor Switches. The binary, trinary and 'modified multilevel converter' (MMC)-based topologies are suitable for varying input sources from solar photo-voltaic (PV). Hence to obtain a 15-level inverter, the existing method requires 28 switches and in binary mode 12 switches are required. In trinary mode with the same level 12 switches, 27 levels can be obtained whereas in MMC only 7 switches are used to carried out the 15 levelsto reduced the harmonic and increase the system efficiency 31 level is required The advantage of these three designs is in the reduction of total harmonic distortion by increasing the levels. Simulations are achieved in MATLAB and comparisons were made.

Keywords- Multilevel inverter, trinary, binary, solar photovoltaic and MMC.

I. INTRODUCTION

Now a days the main drawback in power electronic is switching loss, harmonic and voltage stress in the switch, to overcome the loss we need to add some other Techniques like multilevel inverter to overcome the harmonic problem Multilevel inverter provides a suitable solution for medium and high power systems to synthesize an output voltage which Allows a reduction of harmonic content in voltage and current waveform. The desired multi-staircase output voltage is acquired by combining several dc voltage sources. Solar cells, fuel cells, batteries andultra-capacitors are the most common self-sufficient sources used.

There are three types of multilevel inverter mainly used for reducing harmonics. They are,

- Diode Clamped multilevel inverters
- Flying Capacitor multilevel inverters
- Cascaded H-bridge multilevel inverters

A. **Diode Clamped multilevel inverter**

In multilevel technique the diode clamped inverter play a major role, the diode is mainly used as the clamping device to clamp the dc bus voltage so as to fulfill the steps in the output voltage. This inverter is to use diodes to limit the switching stress and power devices voltage stress. It provides the multiple voltage levels across the different phases to the capacitor banks which are in series. A diode transfers a restricted amount of voltage, thereby reducing the strain on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the important disadvantage of the diode clamped multilevel inverter. This problem can be resolved by increasing the switches, diodes, capacitors. Due to the capacitor balancing issues, these are restricted to the three levels. This type of inverters provides the better efficiency because the fundamental frequency used for all the switching devices and it is a uncomplicated method of the back to back power transfer systems.

B. FLYING CAPACITOR

The formation of this inverter is similar to that of the diode-clamped inverter except that using clamping diodes instead of flying capacitor. The flying capacitor involves the series connection of capacitor clamped switching cells. The capacitors transfer the restricted amount of voltage to electrical devices. In this inverter switching states are same in the diode clamped inverter. Clamping diodes are not needed in this type of multilevel inverters. The output is half of the input DC voltage. It is disadvantage of the flying capacitors multi level inverter. It has the switching redundancy within phase to manage the flaying capacitors. It can manage both the active and reactive power flow. But due to the high switching frequency, switching losses will takes place.

C. **CASCADED MULTILEVEL INVERTER**

The cascaded multi level H-bride inverter topology is to use the capacitors and switches and needs less number of components in each level. This technique consists of series of power conversion cells and power can be simply scaled. The combination of capacitors and switches pair is defined an H-bridge and gives the different input DC voltage for each H-bridge. It contains of H-bridge cells and each cell can supply the three different voltages like zero, positive DC and negative DC voltages. One of the benefit of this type of multi level inverter is that it requires less number of components are compared with diode clamped and flying capacitor inverters. The price and balance of the inverter are less than those of the two inverters. Soft-switching is possible by the some of the new switching methods.

A single-phase multi-string five-level based photo-voltaic (PV) inverter concept for grid-connected Photo Voltaic systems with a pulse width-modulated (PWM) control scheme is proposed in [1]. In that drawback switching loss is high due

to high no switch is used In that [1-3] paper, initially a new concept for sub-multilevel inverter is presented and then series connection of the sub-multilevel inverters is presented as a generalized multilevel inverter, but harmonic is somewhat high. In this[7] paper, a new digital switching technique for cascaded type H bridge multilevel inverter (CMLI) mainly the purpose of this is power quality improvement is proposed in order to ensure an efficient voltage utilization and better harmonic spectrum. And the method presented to control cascaded type multilevel inverter that is implemented with multiple DC sources to get 2n+1-1 levels this process is shown in paper [7-9]. Technique wise good but cost wise high to overcome this type of problem we prefer this type of control technique it is MMC.

In order to increase the efficiency and convert low voltage DC source into usable AC source, the power electronics converters are used to convert the DC to AC. The simulation results presented in this paper verifies the operation of presented MMC topology.

The single phase cascaded design containing some dc sources and switches to reduce the harmonics as shown in Fig.1. A three

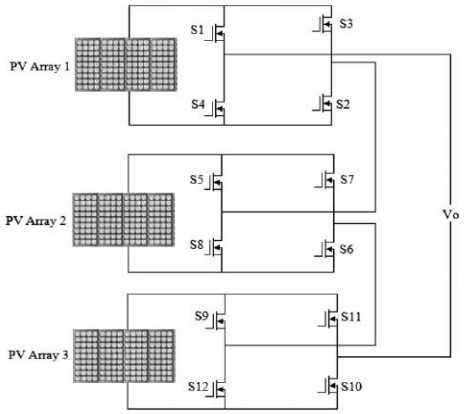

Fig.1:.Circuit Diagram of Binary mode

phase CMI topology is essentially created three identical phase legs of the series-chain of h-bridge converters, which can possibly generate the different types of output voltage waveforms and offers the potential for ac system phase-balancing.

II. SWITCHING STRATEGIES

In conventional approach, PWM techniques are used by the comparison of reference and carrier signals to produce the needed gating signals for the inverter switches. The number of output voltage levelsdeveloped from this approach is given in the following equation,

$$m = 2N_s + 1$$

where m defines the output voltage levels and Ns is the individual inverter stages. The number of switches (l) needed to achieve m levels is given in the following equation,

$$l = 2(m - 1)$$

For the implementation of 15-level CMLI, the number of switches needed is 28 with seven individual inverter stages. In addition to the 28 switches, 182 clamping diodes in case of NPC or diode clamped multilevel inverter and 91 balancing capacitors in case of FC type multilevel inverter along with 14 DC bus capacitors are required to achieve 15-level output. The proposed project deals with the following topologies for the reduction of switches. Improving the number of levels will eventually reduce the harmonic distortion which in turn improves the power quality.

A. BINARY MODE:

In binary cascaded mode operation, the number of levels which can be reached for the given set of inverter stages is given in the following equation,

$$m = 2^{N_s+1} - 1$$

Hence to design a 15-level output, only three inverter stages are needed with 12 switches. To achieve this, a switching circuit with the control scheme incorporating digital logic functions is developed for the solar fed CMLI. The three inverter stages are fed from separate solar PV input source. The input voltages are scaled to the power of 2 in order to achieve the output voltage in the range of 2Ns is shown in FIG1 which can be developed by possible by binary counters. An incremental and descended operator is required to achieve the condition 2Ns + 1 − 1 at the output level.

Table.1. Fifteen level switching pattern in Binary

	Switching Pattern											
Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
7Vdc	1	0	0	1	1	0	0	1	1	0	0	1
6Vdc	1	1	0	0	1	0	0	1	1	0	0	1
5Vdc	1	0	0	1	1	1	0	0	1	0	0	1
4Vdc	1	1	0	0	1	1	0	0	1	0	0	1
3Vdc	1	0	0	1	1	0	0	1	1	1	0	0
2Vdc	1	1	0	0	1	0	0	1	1	1	0	0
1Vdc	1	0	0	1	1	1	0	0	1	1	0	0
0Vdc	1	1	0	0	1	1	0	0	1	1	0	0
-1Vdc	0	1	1	0	1	1	0	0	1	1	0	0
-2Vdc	1	1	0	0	0	1	1	0	1	1	0	0
-3Vdc	0	1	1	0	0	1	1	0	1	1	0	0
-4Vdc	1	1	0	0	1	1	0	0	0	1	1	0
-5Vdc	0	1	1	0	1	1	0	0	0	1	1	0
-6Vdc	1	1	0	0	0	1	1	0	0	1	1	0
-7Vdc	0	1	1	0	0	1	1	0	0	1	1	0

The Table.1 shows the switching pattern of fifteen level by using Binary Mode. The corresponding mode of operations of the cascaded H bridge multilevel inverter stages are described as follows.

a) Maximum output voltage (+7Vs & -7Vs): Active switches S1,S4,S5,S8,S9 and S12 kept in ON and inverter output voltage is 7Vs.

b) Output voltage (+6Vs and -6Vs): Active switches S1,S2,S5,S8,S9 and S12 are kept ON and inverter output voltage is 6Vs.
c) Output voltage (+5Vs and -5Vs): Active switches S1,S4,S5,S6,S9 and S12 are kept ON and inverter output voltage is 5 Vs.
d) Output voltage (+4Vs and -4Vs): Active switches S1,S2,S5,S6,S9 and S10 are kept ON and inverter output voltage is 4Vs.
e) Output voltage (+3Vs and -3Vs): Active switches S1,S4,S5,S8,S9 and S10 are kept ON and inverter output voltage is 3Vs.
f) Output voltage (+2Vs and -2Vs): Active switches S1, S2,S5,S8,S9 and S10 are kept ON and inverter output voltage is 2Vs.
g) Output voltage (+Vs and -Vs): Active switches S1,S4,S5,S6,S9 and S10 are kept ON and inverter output voltage is Vs.
h) Zero output voltage: Active switches S1,S2,S5, S6, S9 and S10 are kept ON and inverter output voltage is Zero.

B.TRINARY MODE:

In trinary mode of operation, the number of levels which can be reached for the given set of inverter stages is given in the following equation,

$$m = 3^{N_s}$$

With the three inverter stages 27 levels can be designed with only 12 switches. To reach this, rather than a digital logic functions used in binary mode, an embedded controller is proposed without the utilization of transformers and complicated algorithms. In this approach, is considered whose input voltages are scaled to the power of illustrates the switching sequence for the switches S1–S12 is shown in FIG1 to obtain 13-level output during the positive half cycle and in negative half cycle the same sequence is rotated by an angle of 90° to achieve the remaining 13 level. By including level zero, the desired 27 levels will be achieved.

Switching Pattern - 27 level

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
13 Vdc	1	0	0	1	1	0	0	1	1	0	0	1
12 Vdc	1	1	0	0	1	0	0	1	1	0	0	1
11 Vdc	0	1	1	0	1	0	0	1	1	0	0	1
10 Vdc	1	0	0	1	1	1	0	0	1	0	0	1
9 Vdc	1	1	0	0	1	1	0	0	1	0	0	1
8 Vdc	0	1	1	0	1	1	0	0	1	0	0	1
7 Vdc	1	0	0	1	0	1	1	0	1	0	0	1
6 Vdc	1	1	0	0	0	1	1	0	0	0	0	1
5 Vdc	0	1	1	0	0	1	1	0	1	0	0	1
4 Vdc	1	0	0	1	1	0	0	1	1	1	0	0
3 Vdc	1	1	0	0	1	0	0	1	1	1	0	0
2 Vdc	0	1	1	0	1	0	0	1	1	1	0	0
1 Vdc	1	0	0	1	1	1	0	0	1	1	0	0
0 Vdc	1	1	0	0	1	1	0	0	1	1	0	0

Table 2: Switching pattern for 27 level - Trinary

The Table.2 shows the twenty seven level switching patterns in Trinary Mode. The corresponding mode of operations of the cascaded H bridge multilevel inverter stages are described as follows.
a) Maximum output voltage (+13Vs & -13Vs): Active switches S1, S4, S5, S8, S9 and S10 kept in ON and inverter output voltage is 13Vs.
b) Output voltage (+12Vs and -12Vs): Active S1, S2, S5, S8, S9 and S12 are kept ON and inverter output voltage is 12Vs.
c) Output voltage (+11Vs and -11Vs): Active switches S2, S3, S5, S8, S9 and S12 are kept ON and inverter output voltage is 11 Vs.
d) Output voltage (+10Vs and -10Vs): Active switches S1, S4, S5, S6, S9 and S12 are kept ON and inverter output voltage is 10Vs.
e) Output voltage (+9Vs and -9Vs): Active switches S1, S2, S5, S6, S9 and S12 are kept ON and inverter output voltage is 9Vs.
f) Output voltage (+8Vs and -8Vs): Active switches S2, S3, S5, S6, S9 and S12 are kept ON and inverter output voltage is 8.
g) Output voltage (+7Vs and -7Vs): Active switches S1, S4, S6, S7, S9 and S12 are kept ON and inverter output voltage is 7Vs.
h) Output voltage (+6Vs and -6Vs): Active switches S1, S2, S6, S7 and S12 are kept ON and inverter output voltage is 6Vs.
i) Output voltage (+5Vs and -5Vs): Active switches S2, S3, S6, S7, S9 and S12 are kept ON and inverter output voltage is 5Vs.
j) Output voltage (+4Vs and -4Vs): Active switches S1, S4, S5, S8, S9 and S10 are kept ON and inverter output voltage is 4Vs.
k) Output voltage (+3Vs and -3Vs): Active switches S1, S2, S5, S8, S9 and S10 are kept ON and inverter output voltage is 3Vs.
l) Output voltage (+2Vs and -2Vs): Active switches S2, S3, S5, S8, S9 and S10 are kept ON and inverter output voltage is 2Vs.
m) Output voltage (+Vs and -Vs): Active switches S1, S4, S5, S6, S9 and S10 are kept ON and inverter output voltage is Vs.
n) Zero output voltage: Active switches S1, S2, S5, S6, S9 and S10 are kept ON and inverter output voltage is Zero.

C. MODIFIED MULTILEVEL INVERTER:

In the above two approaches, the modification is realized in control circuit of CMLI to achieve 15 and 27 levels with three inverter stages. In this approach, the modification is build in both control circuit and predominately in power circuit to obtain 15 levels with only seven switches as shown in Fig.2. The circuit diagram of MMC approach where the input scaling is not mandatory. The addition of diode and Capacitor is to maintain the output within the given interval.
The structure of this topology is based on several modules in which each module consists of a floating capacitor and two switches. This topology is a perfect choice for FACTS applications if the capacitor voltages are maintain in balanced.

MMC is able to transfer the active and reactive power regardless of the load characteristics.

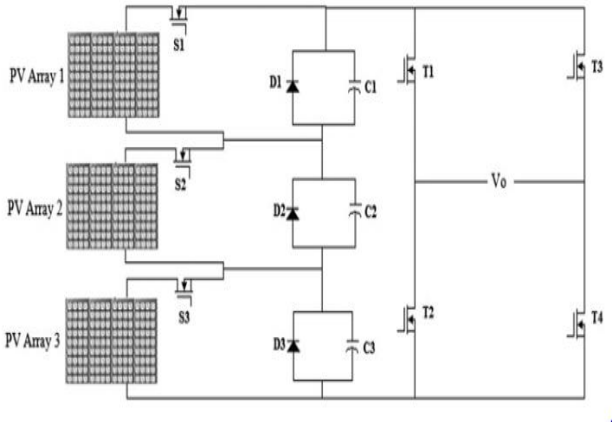

Fig.2: MMC fifteen level circuit

Table3 shows the switching pattern of MMC to reach the 15-level output. Based on the table, the inverter circuit (T1–T4) is in ON condition at all the levels, but the input switches (S1–S3) are managed in such a way that to obtain the needed output voltage. Let the PV array inputs be V1–V3. During the level 1, V1 alone is given as input to the inverter and V2, V3 in OFF condition. Switching Patten of 15-level inverter is show in table1 similarly the 15 level is achieved by controlling the ON/OFF status of the input voltages.

Switching Pattern - 15 level							
Level	S1	S2	S3	S4	S5	S6	S7
7 Vdc	1	1	1	1	0	0	1
6 Vdc	0	1	1	1	0	0	1
5 Vdc	1	0	1	1	0	0	1
4 Vdc	0	0	1	1	0	0	1
3 Vdc	1	1	0	1	0	0	1
2 Vdc	0	1	0	1	0	0	1
1 Vdc	1	0	0	1	0	0	1
0 Vdc	0	0	0	0	0	0	0
-1 Vdc	1	0	0	0	1	1	0
-2 Vdc	0	1	0	0	1	1	0
-3 Vdc	1	1	0	0	1	1	0
-4 Vdc	0	0	1	0	1	1	0
-5 Vdc	1	0	1	0	1	1	0
-6 Vdc	0	1	1	0	1	1	0
-7 Vdc	1	1	1	0	1	1	0

Table.3. Fifteen level Switching Pattern - MMC

The Table.3 shows the switching pattern of fifteen levels by using MMC Mode. The corresponding mode of operations of the cascaded H bridgefifteen level inverter stages are described as follows.

a) Maximum output voltage (+7Vs & -7Vs): Active switches S1,S2,S3,S4 and S7 kept in ON and inverter output voltage is 7Vs.

b) Output voltage (+6Vs and -6Vs): Active switches S2,S3,S4 and S7 are kept ON and inverter output voltage is 6Vs.

c) Output voltage (+5Vs and -5Vs): Active switches S1,S3,S4 and S7 are kept ON and inverter output voltage is 5 Vs.

d) Output voltage (+4Vs and -4Vs): Active switches S3,S4 and S7 are kept ON and inverter output voltage is 4Vs.

e) Output voltage (+3Vs and -3Vs): Active switches S1,S2,S4 and S7 are kept ON and inverter output voltage is 3Vs.

f) Output voltage (+2Vs and -2Vs): Active switches S2, S4 and S7 are kept ON and inverter output voltage is 2Vs.

g) Output voltage (+Vs and -Vs): Active switches S1,S4 and S7 are kept ON and inverter output voltage is Vs.

h) Zero output voltage: All switches are kept OFF and inverter output voltage is Zero.

D. PROPOSED MODIFIED MULITLEVEL CONNECTIONS (MMC):

In this project, the techniques include 'binary', 'trinary' and modified multilevel connections' (MMCs) has to be designed and analyzed which converter gives the better power quality. The four stages CMLI power circuit used to achieve 15 levels by 'binary' mode using digital switching technique composes of counters and logic functions. The same power circuit is used to achieve 27 levels by using 'trinary' mode. In MMC, a 31 level is achieved with the single stage inverter by addition of input voltages using the embedded controller based on the proposed switching sequence. The comparison of three methods with the existing techniques are analyzed and experimentally verified. The block diagram of this proposed MMC is shown in Fig.3.

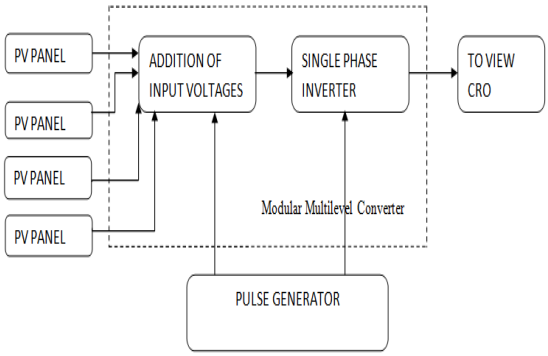

Fig.3: Block Diagram of proposed MMC

The formation of this topology is based on several modules in which each module consists of a floating capacitor, a diode and a switch as shown in Fig.4. A solar PV panel is modeled by the interconnection of solar cells in series and parallel to achieve the required rating. The input supply is feed through PV module as a dc source and this output voltage magnitude is increase to require level to obtain the line voltage is employed. The output of the DC power from the PV panel supplied to the modular multilevel DC/AC power converter. A Pulse Generator generates the control signals or firing pulse for the inverter to maintain the level output.

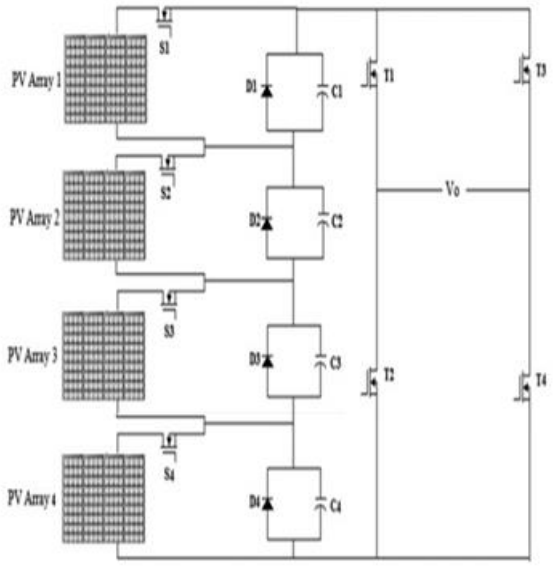

Fig.4. Proposed thirty one level MMC

	Switching Pattern - 31 levels							
Level	S1	S2	S3	S4	S5	S6	S7	S8
15 Vdc	1	1	1	1	1	0	0	1
14 Vdc	0	1	1	1	1	0	0	1
13 Vdc	1	0	1	1	1	0	0	1
12 Vdc	0	0	1	1	1	0	0	1
11 Vdc	1	1	0	1	1	0	0	1
10 Vdc	0	1	0	1	1	0	0	1
9 Vdc	1	0	0	1	1	0	0	1
8 Vdc	0	0	0	1	1	0	0	1
7 Vdc	1	1	1	0	1	0	0	1
6 Vdc	0	1	1	0	1	0	0	1
5 Vdc	1	0	1	0	1	0	0	1
4 Vdc	0	0	1	0	1	0	0	1
3 Vdc	1	1	0	0	1	0	0	1
2 Vdc	0	1	0	0	1	0	0	1
1 Vdc	1	0	0	0	1	0	0	1
0 Vdc	0	0	0	0	0	0	0	0
- 1 Vdc	1	1	1	1	0	1	1	0
- 2 Vdc	0	1	1	1	0	1	1	0
- 3 Vdc	1	0	1	1	0	1	1	0
- 4 Vdc	0	0	1	1	0	1	1	0
- 5 Vdc	1	1	0	1	0	1	1	0
- 6 Vdc	0	1	0	1	0	1	1	0
- 7 Vdc	1	0	0	1	0	1	1	0
- 8 Vdc	0	0	0	1	0	1	1	0
- 9 Vdc	1	1	1	0	0	1	1	0
- 10 Vdc	0	1	1	0	0	1	1	0
- 11 Vdc	1	0	1	0	0	1	1	0
-12 Vdc	0	0	1	0	0	1	1	0
-13 Vdc	1	1	0	0	0	1	1	0
- 14 Vdc	0	1	0	0	0	1	1	0
- 15 Vdc	1	0	0	0	0	1	1	0

Table.4. MMC 31 level Switching Pattern

The Table.4 shows the switching pattern of thirty one levels by using MMC Mode. The corresponding mode of operations of the cascaded H bridgethirty one level inverter stages are described as follows.

a) Maximum output voltage (+15Vs & -15Vs): Active switches S1, S2, S3, S4, S5and S8 kept in ON and inverter output voltage is 15Vs.

b) Maximum output voltage (+14Vs & -14Vs): Active switches S2, S3, S4, S5and S8 kept in ON and inverter output voltage is 14Vs.

c) Maximum output voltage (+13Vs & -13Vs): Active switches S1, S3, S4, S5and S8 kept in ON and inverter output voltage is 13Vs.

d) Output voltage (+12Vs and -12Vs): Active switches, S3, S4, S5and S8 are kept ON and inverter output voltage is 12Vs.

e) Output voltage (+11Vs and -11Vs): Active switches S1, S2, S4, S5and S8 are kept ON and inverter output voltage is 11 Vs.

f) Output voltage (+10Vs and -10Vs): Active switches S2, S4, S5 and S8 are kept ON and inverter output voltage is 10Vs.

g) Output voltage (+9Vs and -9Vs): Active switches S1, S4, S5 and S8 are kept ON and inverter output voltage is 9Vs.

h) Output voltage (+8Vs and -8Vs): Active switches S4, S5 and S8 are kept ON and inverter output voltage is 8.

i) Output voltage (+7Vs and -7Vs): Active switches S1, S2, S3, S5 and S8 are kept ON and inverter output voltage is 7Vs.

j) Output voltage (+6Vs and -6Vs): Active switches S2, S3, S5and S8 are kept ON and inverter output voltage is 6Vs.

k) Output voltage (+5Vs and -5Vs): Active switches S1, S3, S5 and S8 are kept ON and inverter output voltage is 5Vs.

l) Output voltage (+4Vs and -4Vs): Active switches S3, S5 and S8 are kept ON and inverter output voltage is 4Vs.

m) Output voltage (+3Vs and -3Vs): Active switches S1, S2, S5 and S8 are kept ON and inverter output voltage is 3Vs.

n) Output voltage (+2Vs and -2Vs): Active switches S2,S5 and S8 are kept ON and inverter output voltage is 2Vs.

o) Output voltage (+Vs and -Vs): Active switches S1, S5 and S8 are kept ON and inverter output voltage is Vs.

p) Zero output voltage: All Active switches S1, S2, S3, S4, S5, S6, S7and S8 are kept OFF and inverter output voltage is Zero.

III. SIMULATION RESULTS

The simulation results and the corresponding harmonics analysis for all the three topologies are achieved in MATLAB. The model of solar PV panel is needred which serves as the input for the proposed inverter. Because now a day's renewable energy act the major role in electricity. The input is given from the DC supply and analysis were made and also most of the solar PV models proposed tends to the estimation of its characteristics and MPP tracking is used to reached the desired power A solar PV panel is modeled by the interconnection of solar cells in series and parallel to achieve the required rating of 48 V, 7 A is shown in FIG: 4 and. Each solar cell of rating (0.5 V, 7 A) with 96 numbers is connected in series at standard test conditions of 2000 W/mm2 and 25°C. it is show in the FIG:3 output of the solar voltage in corresponding to four panel which is 47v ,96v,191v and 382v.

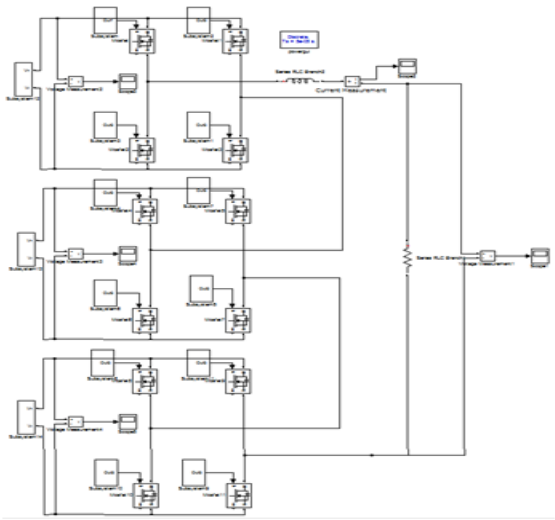

Fig.5: fifteen level inverter – Binary Mode

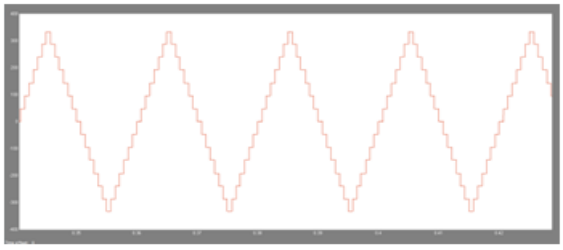

Fig.6: Fifteen level output voltage -Binary Mode

The fifteen level circuit diagram and simulation results are shown in above Fig.5 and Fig.6.

The trinary Mode simulation results of twenty seven level as shown in below. The output voltage of twenty seven level as shown in Fig.7.

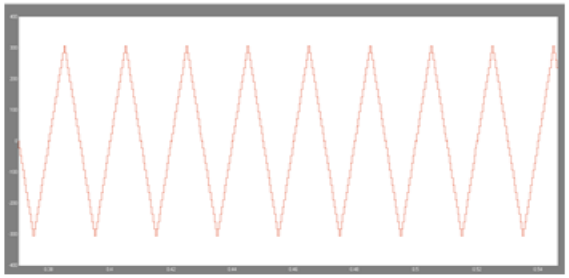

Fig.7: Twenty seven level output voltage – Trinary Mode

The current waveform of twenty seven level as shown in Fig.8.

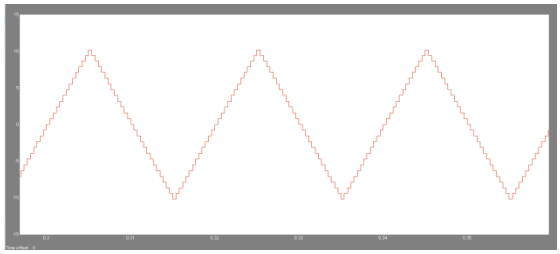

Fig.8: Current waveform of twenty seven levels

The total harmonic distortion of twenty seven level by using Trinary concept as shown in below Fig.9.

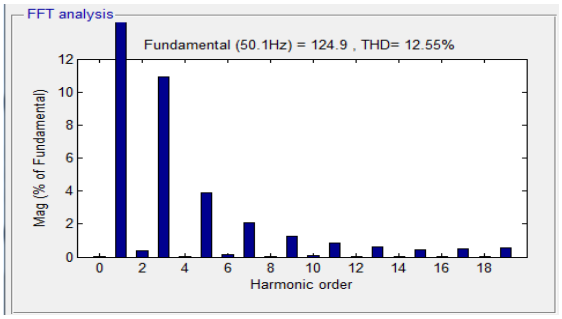

Fig.9: THD – 27 level

The fifteen level MMC circuit diagram as shown in below Fig.10.

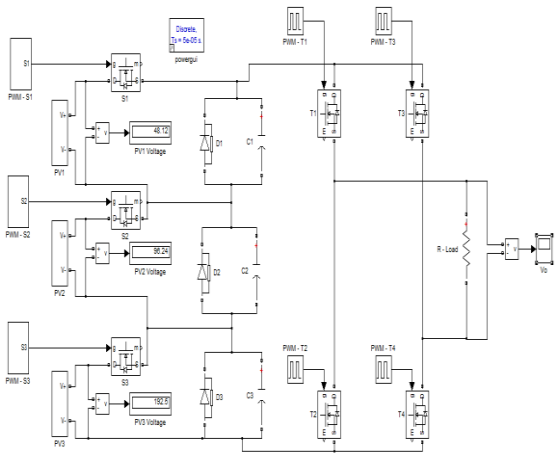

Fig.10: Fifteen level circuit of MMC

The fifteen level MMC converter output voltage is shown in Fig.11.

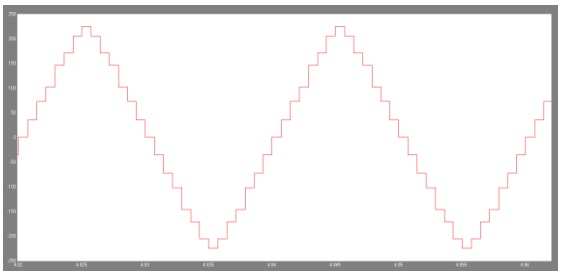

Fig.11: MMC fifteen level output voltage

The Total harmonic distortion value of fifteen level output voltage is shown in Fig.12.

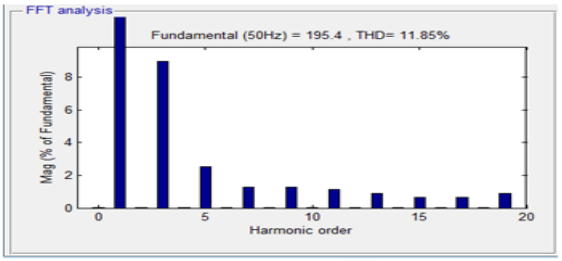

Fig.12: THD value for 15 level MMC

The proposed MMC thirty one level circuit diagram as shown in below Fig.13.

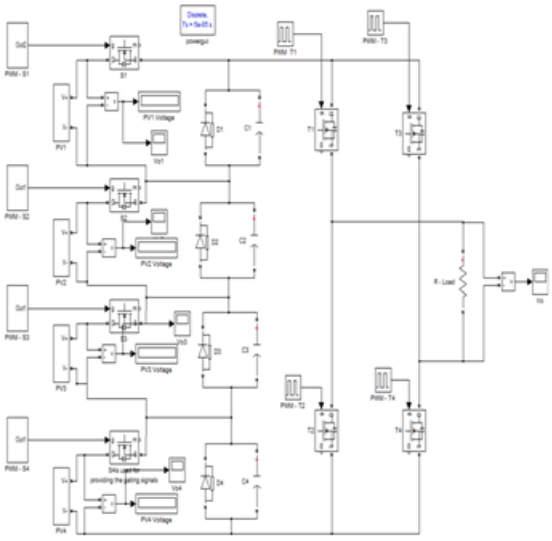

Fig.13: Proposed 31 levels simulation circuit Diagram – MMC Mode

The solar panel input voltage for each panel as shown in Fig.14.

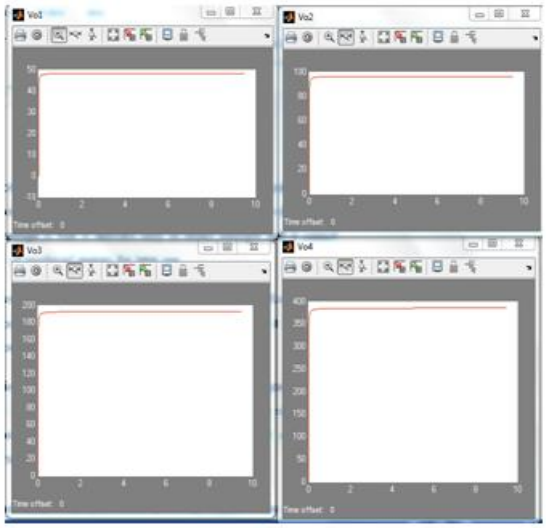

Fig.14: Each panel Input Voltage of MMC

The output voltage waveform of thirty one level by using MMC as shown in below Fig.15.

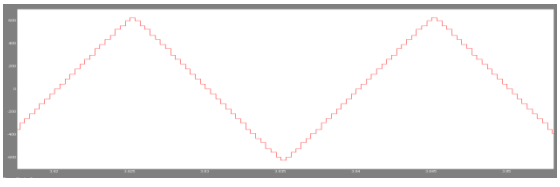

Fig.15: Thirty one level output voltage – MMC Mode

The total harmonic distortion of thirtyone level by using MMC concept as shown in below Fig.16.

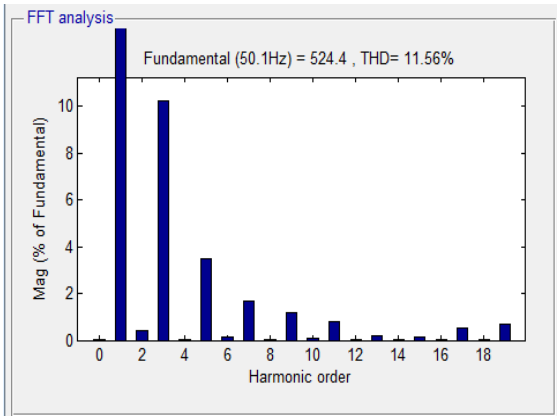

Fig.16: THD – 31 level

IV. CONCLUSION

A fifteen level solar fed cascaded multilevel inverter for the elimination of certain harmonic orders is developed for the power quality improvement. The method is compared with the conventional PWM approach, which shows that OHSW based method is much suitable and an ideal choice for implementing selective harmonic elimination cases. The advantages of this method include simple computational algorithm and no requirement of filters, detailed look up tables and output transformers. Moreover, this technique can be implemented in both standalone and grid interacted PV systems.

V. REFERENCE PAPERS

[1]. Rahim, N.A., Selvaraj, J.: 'Multistring five-level inverter with novelPWM control scheme for PV application', IEEE Trans. Ind. Electron.,2010, 57, (6), pp. 2111–2123

[2]. Selvaraj, J., Rahim, N.A.: 'Multilevel inverter for grid-connected PVsystem employing digital PI controller', IEEE Trans. Ind. Electron.,2009, 56, (1), pp. 149–158

[3]. Rahim, N.A., Chaniago, K., Selvaraj, J.: 'Single-phase seven-levelgrid-connected inverter for photovoltaic system', IEEE Trans. Ind.Electron., 2011, 58, (6), pp. 2435–2443

[4]. Barbosa, P.G., Braga, H.A.C., do Carmo Barbosa Rodrigues, M.,Teixeira, E.C.: 'Boost current multilevel inverter and its application onsingle-phase grid-connected photovoltaic systems', IEEE Trans.Power Electron., 2006, 21, (4), pp. 1116–1124

[5]. Villanueva, E., Correa, P., Rodríguez, J., Pacas, M.: 'Control of asingle-phase cascaded H-bridge multilevel inverter for grid-connectedphotovoltaic systems', IEEE Trans. Ind. Electron., 2009, 56, (11),pp. 4399–4406

[6]. Kangarlu, M.F., Babaei, E.: 'A generalized cascaded multilevel inverterusing series connection of sub multilevel inverters', IEEE Trans. PowerElectron., 2013, 28, (2), pp. 625–636

[7]. Nami, A., Zare, F., Ghosh, A., Blaabjerg, F.: 'A hybrid cascadeconverter topology with series-connected symmetrical andasymmetrical diode-clamped H-bridge cells', IEEE Trans. PowerElectron., 2011, 26, (1), pp. 51–65

[8]. Mondal, G., Gopakumar, K., Tekwani, P.N., Levi, E.: 'A reducedswitch-count five-level inverter with common-mode

voltageelimination for an open-end winding induction motor drive', IEEETrans. Ind. Electron., 2007, 54, (4), pp. 2344–2351
[9]. Babaei, E.: 'Optimal topologies for cascaded sub-multilevel converters',J. Power Electron., 2010, 10, (3), pp. 251–261
[10]. Babaei, E.: 'A cascade multilevel converter topology with reducednumber of switches', IEEE Trans. Power Electron., 2008, 23, (6),
pp. 2657–2664
[11]. Babaei, E., Hosseini, S.H., Gharehpetian, G.B., Haque, M.T., Sabahi,M.: 'Reduction of DC voltage sources and switches in asymmetricalmultilevel converters using a novel topology', J. Electr. Power Syst.Res., 2007, 77, (8), pp. 1073–1085
[12]. Dixon, J., Pereda, J., Castillo, C., Bosch, S.: 'Asymmetrical multilevelinverter for traction drives using only one DC supply', IEEE Trans.Veh. Tech., 2010, 59, (8), pp. 3736–3743
[13]. Rotella, M., Penailillo, G., Pereda, J., Dixon, J.: 'PWM method toeliminate power sources in a non-redundant 27-level inverter formachine drive applications', IEEE Trans. Ind. Electron., 2009, 56, (1),pp. 194–201
[14]. Dixon, J., Mor´an, L.: 'High-level multistep inverter optimization using aminimum number of power transistors', IEEE Trans. Power Electron.,2006, 21, (2), pp. 330–337
[15]. Kang, F.-S., Park, S.-J., Lee, M.H., Kim, C.-U.: 'An efficientmultilevel-synthesis approach and its application to a 27-levelinverter', IEEE Trans. Ind. Electron., 2005, 52, (6), pp. 1600–1606
[16]. Dixon, J., Bretón, A.A., Ríos, F.E., Rodríguez, J., Pontt, J., Pérez, M.A.:'High-power machine drive, using nonredundant 27-level inverters andactive front end rectifiers', IEEE Trans. Power Electron., 2007, 22, (6),
pp. 2527–2533
[17]. Cecati, C., Ciancetta, F., Siano, P.: 'A multilevel inverter forphotovoltaic systems with fuzzy logic control', IEEE Trans. Ind.Electron., 2010, 57, (12), pp. 4115–4125
[18]. Beser, E., Arifoglu, B., Camur, S., Beser, E.K.: 'Design and applicationof a single phase multilevel inverter suitable for using as a voltageharmonic source', J. Power Electron., 2010, 10, (2), pp. 138–145
[19]. Soon, J.J., Low, K.-S.: 'Photovoltaic model identification using particleswarm optimization with inverse barrier constraint', IEEE Trans. PowerElectron., 2012, 27, (9), pp. 3975–3983
[20]. Tsai, H.-L., Tu, C.-S., Su, Y.-J.: 'Development of generalizedphotovoltaic model using MATLAB/Simulink'. Proc. World Congresson Engineering and Computer Science, San Francisco, USA, October2008

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