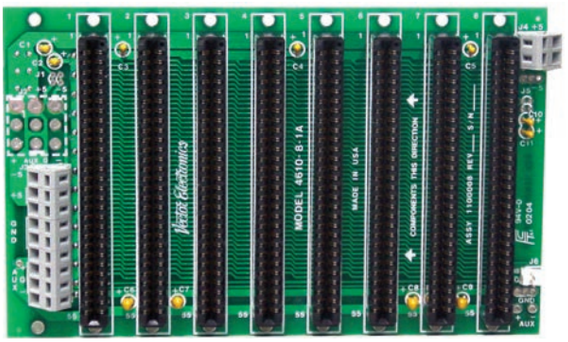
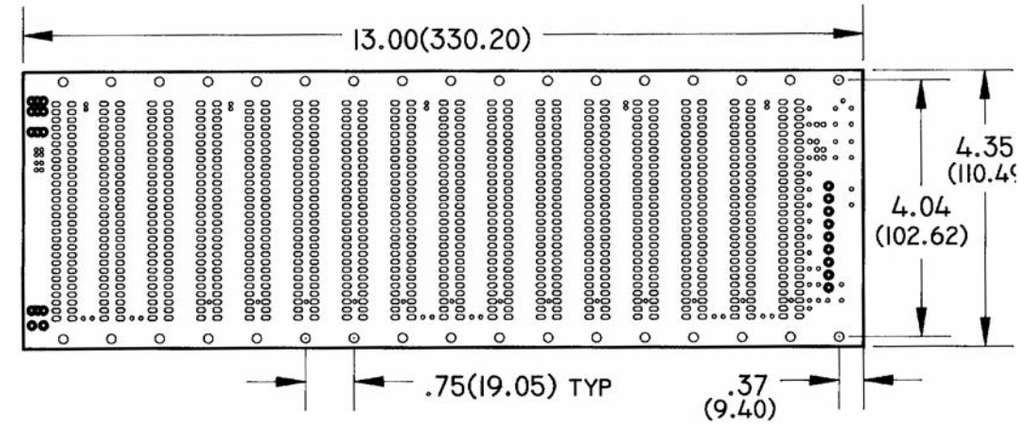
STD Bus, 8 & 16 Slots



Model 4610-8-1A 8-slot STD Backplane

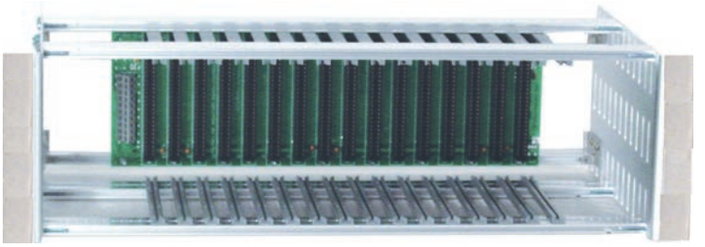
Vectorboard® STD Bus industrial backplanes per IEEE 961 microcomputer bus, compact and rugged are fully assembled and tested. Designed for 4.5" X 6.5" plug-in boards, Vector STD Bus backplanes are available in 8 or 16-slots. Optional integration with VectorPak™ CCA13-series subracks listed below. Speed capability up to 10MHz; 2-layer design. Ample positions for decoupling capacitors; interrupt priority lines.

- Faraday shield lines reduce cross-talk
- Wiring pads on board to connect RESET switch for front panel controls
- High reliability connectors with gold/plated contacts
- 10-position power connector
- Wago power blocks
- STDbus pin-out provided with IN313 data sheet



Specifications:

Material	FR4 Epoxy Glass. .062" thick, UL94-V-0 compliant
Operating Temp.:	0°to 60°C
Storage:	-20 to 60°C
Rel. Humidity:	0-95%, non-condensing



CCA13S-16/90 Subrack Kit
with 16-slot STD backplane (shown assembled)

Backplane Part No.	Description	Backplane Dimensions Width	Length	Thickness	Connector Spacing	Plugbord Series	Accessories Extender	Assemblies w/ Cardrack
4610-8-1A	8-slot	4.35"	7.00"	1/16"	.750"	4610 Series	3690-16	CCA13S-8/90 CCA13S-HT8/90
4610-16-1A	16-slot	4.35"	13.00"	1/16"	.750"	4610 Series	3690-16	CCA13S-16/90

4610-8, 4610-16 SERIES STD BUS MOTHERBOARD

1.0 GENERAL

Vectors' 4610-8 and -16 motherboards are state-of-the-art design. These motherboards are exceptionally quiet, fast, and reliable and are designed for up to 10 MHz operation. Full Faraday shielding of all signal traces, and heavy power buses with extensive capacitive by-passing, exemplify the design.

These motherboards fit Vector Electronic's variety of desktop and rack mount card cages and enclosures. Insulating mounting spacers are provided. The connector positions for plug-in boards are spaced on 0.75" centers which is the most popular and useful STD Bus option.

These boards have circuit pads for mounting decoupling capacitors on the +5 volt buses and on the auxiliary +12 volt buses as noted later. The power and ground buses have superior current carrying capacity. The signal lines are run between Faraday shield lines which are ground lines that "stub-out" and "dead end" from each ground cross-tie bus. On the opposite side of the board there is also a ground line position exactly opposite to each signal line. This gives a partial wave guide effect, to shield the signal on each line from every other line. Note that the signal lines pass through the plated holes and alternate from component side to non-component side of the board as the line progresses from connector to connector. This is a key factor in obtaining this superior shielding for a "quiet" motherboard operation.

A green epoxy solder mask is applied over all conductors except at connection pads. This protects against solder bridging between adjacent circuits. The epoxy is tough, but avoid scratching it with sharp items or hot soldering iron. The plated connector holes are 0.033" diameter and facilitate easy, good quality solder joints on connectors with solder type leads. Connector leads with 0.025" square wrap-posts (0.035" diagonal) will not fit into these holes.

Active termination can be "added" to these motherboards if desired, by using Vector's 4610-6 plug-in combination board with etched circuits for active termination, card extension, and built-in Logic probe.

2.0 MOUNTING MOTHERBOARDS IN VECTOR CARD CAGES OR ENCLOSURES

Motherboards are mounted in Vector cages and enclosures by mounting against the narrow edge of the upperand lower struts provided. These struts are adjustable up-and-down and fore-and-aft so as to allow proper positioning of the motherboard relative to the daughter cards in the card guides. These struts have grooves in the narrow edge into which threaded studs are inserted. These studs should be positioned to match every other hole in the motherboard, starting at one end. Vector provides either individual round insulating spacers to be put over each stud or else two insulating strips,one for each strut, and these should be mounted so as to isolate the solder side of the motherboard from the metal strut even though it is insulated by anodizing. Install the motherboard over the studs causing the studs to pass through the motherboard and through the connector mounting ears. Then place flat washer, lock washer and nut on stud and tighten. Check that no component leads protrude to mounting strut. Insert cards into card guides of cage and loosen and reposition the two mounting struts holding the motherboard so as to bring the motherboard into correct elevation and depth location to engage the daughterboards in the card guides. Engage a daughterboard to the motherboard at each end of the motherboard and in the center of the motherboard and then check for proper depth position of the daughterboard for proper card extraction. Tighten the mounting struts of the motherboard and installation is then complete. If electrical interconnection wiring was not previously terminated, then it should be done so now after checking with an ohmmeter that there is no continuity between +5 volt and ground buses and between auxiliary +12 and auxiliary ground buses.

NOTE: The STD motherboard edge connectors are centered, and will allow boards to be inserted backwards. This should be avoided at all times and may cause board damage. The component side of the STD cards face J2 power connector. The motherboard connectors can be polarized with the provided plastic polarizing keys by installing between pins 26 and 28, or 25 and 27. Many STD cards already have key slots to accommodate these polarizing keys.

3.0 POWER SUPPLY AND RESET SWITCH

Power corrections to the Vector 4610- motherboards are made through a "quick release" terminal strip. The terminal strip is designed to accept AWG 24 to 14 wire sizes. Wire should be stripped to a length of .195 to .230 inches (5 to 6 mm), and inserted into the terminal using the installation tool provided.

CAUTION: Wire should not to be tinned (solder coated). Quick release spring clamp terminals are designed for use with stranded wire which is not tinned. A poor connection will result from the use of tinned wire connections.

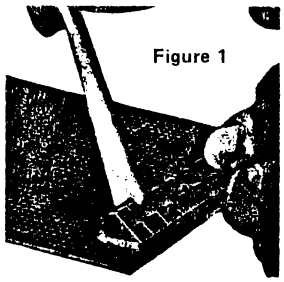


Figure 1

A normally open, external momentary RESET switch may be connected to the RESET and GND pins on J5.

4.0 PRIORITY INTERRUPT FUNCTION

All bus lines are continuous except pin 51 PCO (priority chain out), and pin 52 PCI (priority chain in). Refer to "STD Bus Specification and Practice" bulletin from STD manufacturing group, issued by Pro-log for accurate detailed information on priority system operation. **Figure 2** shows that pin 51 PCO of the higher priority board location, connects through the motherboard to pin 52 PCI of the next lower priority board location. Note that non-prioritized daughterboards have jumper circuits to continue the chain. The prioritized I/O board in the receptacle closest to the CPU board (or seperate interrupt board) has the highest priority. Note also that if a receptacle position is left unused, then a jumper would be required to continue the priority chain, if desired. Vector's 3 function 4610-6 extender, active terminator and Logic Probe combination board, has a switch circuit to accommodate active priority chain systems when trouble shooting.

The STD Bus pinout is organized into five functional groups. The organization and pinouts are shown in **Figure 3.** This figure gives the mnemonic function and signal flow direction (referenced to the processor card in control of the Bus) for each pin of the STD Bus. The STD Bus is further defined as requiring a 56-pin (dual 28) card edge connector with 0.125 inch pin centers. The connectors accept the standard 4½" x6½" x 0.062" card.

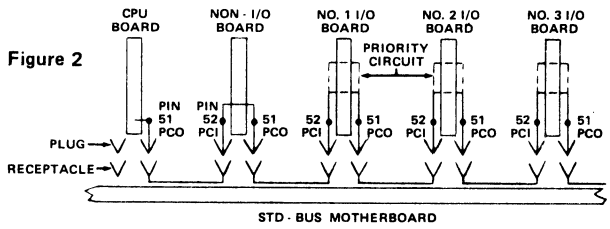


Figure 2

		COMPONENT SIDE				CIRCUIT SIDE			
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5VDC	In	Logic Power (bussed)	2	+5VDC	In	Logic Power (bussed)
	3	GND	In	Logic Ground (bussed)	4	GND	In	Logic Ground (bussed)
	5	VBB #1	In	Logic Bias #1 (-5V)	6	VBB #2	In	Logic Bias #2 (-5V)
DATA BUS	7	D3	In/Out	Low-Order Data Bus	8	D7	In/Out	High-Order Data Bus
	9	D2	In/Out	Low-Order Data Bus	10	D6	In/Out	High-Order Data Bus
	11	D1	In/Out	Low-Order Data Bus	12	D5	In/Out	High-Order Data Bus
	13	D0	In/Out	Low-Order Data Bus	14	D4	In/Out	High-Order Data Bus
ADDRESS BUS	15	A7	Out	Low-Order Address Bus	16	A15	Out	High-Order Address Bus
	17	A6	Out	Low-Order Address Bus	18	A14	Out	High-Order Address Bus
	19	A5	Out	Low-Order Address Bus	20	A13	Out	High-Order Address Bus
	21	A4	Out	Low-Order Address Bus	22	A12	Out	High-Order Address Bus
	23	A3	Out	Low-Order Address Bus	24	A11	Out	High-Order Address Bus
	25	A2	Out	Low-Order Address Bus	26	A10	Out	High-Order Address Bus
	27	A1	Out	Low-Order Address Bus	28	A9	Out	High-Order Address Bus
	29	A0	Out	Low-Order Address Bus	30	A8	Out	High-Order Address Bus
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Push-Button Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	53	AUX GND	In	AUX Ground (bussed)	54	AUXGND	In	AUX Ground (bussed)
	55	AUX +V	In	AUX Positive (+12V DC)	56	AUX -V	In	AUX Negative (-12V DC)

*Low-level active indicator

Figure 3

STD Bus Pin Assignments

STD BUS (IEEE961) COMPONENT SIDE				
	PIN	MNEMONIC	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	+5VDC	In	Logic Power (bussed)
	3	GND	In	Logic Ground (bussed)\
	5	VBB#1	In	Logic Bias #1 (-5V)
DATA BUS	7	D3	In/Out	Low-Order Data Bus
	9	D2	In/Out	Low-Order Data Bus
	11	D1	In/Out	Low-Order Data Bus
	13	D0	In/Out	Low-Order Data Bus
	15	A7	Out	Low-Order Address Bus
	17	A6	Out	Low-Order Address Bus
	19	A5	Out	Low-Order Address Bus
ADDRESS BUS	21	A4	Out	Low-Order Address Bus
	23	A3	Out	Low-Order Address Bus
	25	A2	Out	Low-Order Address Bus
	27	A1	Out	Low-Order Address Bus
	29	A0	Out	Low-Order Address Bus
	31	WR*	Out	Write to Memory or I.O.
	33	IORQ*	Out	I/O Address Select
	35	IOEXP*	In/Out	I/O Expansion
	37	REFRESH*	Out	Refresh Timing
CONTROL BUS	39	STATUS 1*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge
	43	INTAK*	Out	Interrup Acknowledge
	45	WAITRQ*	In	Wait Request
	47	SYSRESET*	Out	System Reset
	49	CLOCK*	Out	Clock from Processor
	51	PCO	Out	Priority Chain Out
AUXILIARY POWER BUS	53	AUG GND	In	AUX Ground (bussed)
	55	AUX+V	In	AUX Positive (+12V DC)
CIRCUIT SIDE				
LOGIC POWER BUS	2	+5VDC	In	Logic Power (bussed)
	4	GND	In	Logic Ground (bussed)
	6	VBB#2	In	Logic Bias #2 (-5V)
DATA BUS	8	D7	In/Out	High-Order Data Bus
	10	D6	In/Out	High-Order Data Bus
	12	D5	In/Out	High-Order Data Bus
	14	D4	In/Out	High-Order Data Bus
	16	A15	Out	High-Order Data Bus
	18	A14	Out	High-Order Data Bus
	20	A13	Out	High-Order Data Bus
ADDRESS BUS	22	A12	Out	High-Order Data Bus
	24	A11	Out	High-Order Data Bus
	26	A10	Out	High-Order Data Bus
	26	A9	Out	High-Order Data Bus
	30	A8	Out	High-Order Data Bus
	32	RD*	Out	Read Memory or I.O.
	34	MEMRQ*	Out	Memory Address Select
	36	MEMRX	In/Out	Memory Expansion
	38	MCSYNC*	Out	CPU Machine Cycle Sync.
CONTROL BUS	40	STATUS 0*	Out	CPU Status
	42	BUSRQ*	In	Bus Request
	44	INTRQ*	In	Interrup Request
	46	NMIRQ*	In	Nonmaskable Interrupt
	48	PBRESET*	In	Push-Button Reset
	50	CNTROL*	In	AUX Timing
	52	PCI	In	Priority Chain In
AUXILIARY POWER BUS	54	AUG GND	In	AUX Ground (bussed)
	56	AUX-V	In	AUX Positive (-12V DC)