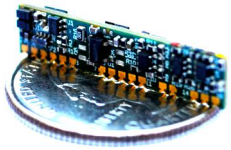
100X, 100L, 100T
GaN Controller Module
Power Sequencer, Non-Inverting Analog Input



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PRODUCT FLYER
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General Description

The 100 Series GaN Controller is capable of operating and protecting all depletion-mode transistors. The non-inverting analog input accepts negative voltage to produce buffered negative gate bias. It allows 360° board placement with little or no line crossovers in the main board. A single power supply is enough for the 100 to provide dynamic control. Little or no filtering is needed in heavy RF environments. The 100 works seamlessly with 300 and 400 Series MOS switches that have compact footprints for locating near the transistor drain choke. It comes in evaluation boards that are ideal for fast prototyping.

Features

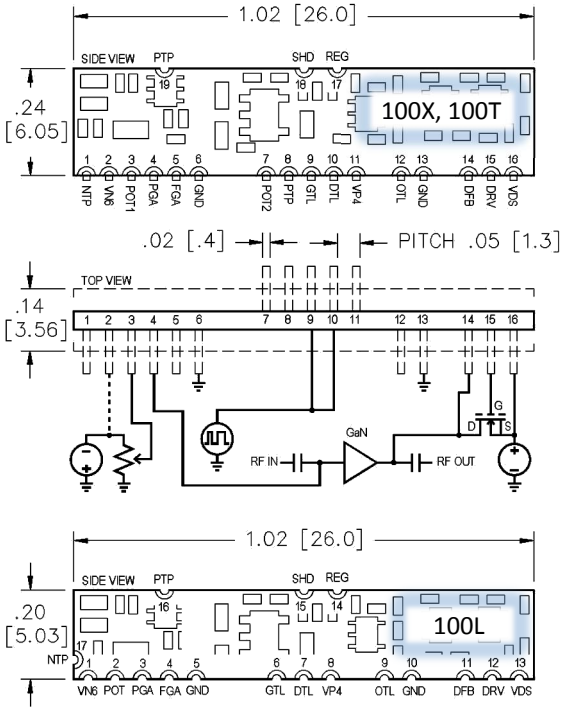
- Protects GaN devices from any power sequence of voltage supplies.
- Internal Negative voltage with 30mA OR external supply for 100mA boost.
- Bias Voltage has Fixed Gate OR Pulsed Gate configuration.
- Simultaneous Gate-Drain sequencing OR Independent Gate/Drain control.
- TTL OR Open Drain (<300mA) output drive for MOSFET switches.
- Temp compensation from local OR remote temp sensor feedback.
- >25dB EMI/RFI Rejection at all I/O ports except from auxiliary taps.
- <500 nsec total delay from V_Logic to V_Drain with applicable switch.
- RoHS* Compliant

Specification Snapshot

Parameter	Min	Max
Supply (+) Voltage	+20 V	+65 V
Supply (-) Voltage, Optional	-6 V	0 V
TTL Voltage Logic High	+3.6 V	+5.0 V
TTL Voltage Logic Low	0 V	+1.4 V
Internal (-) Supply V, Gate Pinchoff	-4.3 V	
Internal (-) Supply I	-30 mA	
Gate Bias Voltage Range	-4.3V	-0.5 V
Out Switch Drive, Open Drain (V)	0 V	+60 V
Out Switch Drive, Open Drain (I)		300 mA
Output ON Prop Delay (T_Delay 1)		120 ns
Output ON Fall Time (T_Fall 1)		120 ns
Output OFF Prop Delay (T_Delay 5)		80 ns
Output OFF Rise Time (T_Rise 3)		80 ns
Gate ON Prop Delay (T_Delay 3)		160 ns
Gate ON Rise Time (T_Rise 2)		60 ns
Gate OFF Prop Delay (T_Delay 4)		160 ns
Gate OFF Fall Time (T_Fall 2)		60 ns
Soldering Temp (10 sec)		+260°C
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C

Propagation Delay is measured from 90% of TTL to 10% of Open Drain Output with pull-up resistor. Rise/Fall Times are measured at 10% and 90% of signal. Both measurements are summed for total time.

Typical Connection Diagram



LABEL	PIN 100X 200X	PIN 100L 200L	DESCRIPTION
NTP	1	17	Aux Negative Voltage Tap
VN6	2	1	Optional Neg (-) Supply
POT	3	2	Gate Voltage Input Adjust
PGA	4	3	Pulsed Gate Voltage Out
FGA	5	4	Fixed Gate Voltage Out
GND	6	5	Ground
POT	7		Connected to Pin 3
PTP	8		Aux Positive Voltage Tap
GTL	9	6	Gate Pulse Logic Enable
DTL	10	7	Drain Pulse Logic Enable
VP4	11	8	Optional Logic (+) Supply
OTL	12	9	Active-Low TTL Driver
GND	13	10	Ground
DFB	14	11	MOS Drain Feedback
DRV	15	12	Open Drain MOS Driver
VDS	16	13	High Voltage Supply
REG	17	14	Aux Regulator Output
SHD	18	15	Aux Gate Threshold Adj
PTP	19	16	Aux Positive Voltage Tap

Ordering Information

Model ^	
100_02R6 100_02R0 100_01R4 100_00R8	UNIVERSAL GaN CONTROLLER: NEGATIVE ANALOG INPUT, SINGLE DC SUPPLY, VGS SHUTDOWN AT -2.6V THRU -0.8V**. INDEPENDENT OR SEQUENTIAL SWITCHING OF DRAIN AND GATE
120_02R6 120_02R0 120_01R4 120_00R8	DRAIN CONTROLLER: 100_ WITH NO GATE SWITCHING CAPABILITY
124_02R6 124_02R0 124_01R4 124_00R8	BASIC SEQUENCER: 100_ WITH NO GATE SWITCHING, NO INTERNAL NEGATIVE AND LOGIC (+5V) SUPPLIES

^ Select type X, L, or T
** All models have provisions for adjusting Vgs shutdown threshold to desired level.

100T, Optional Pins | 100X, Standard | 100L, Low Profile

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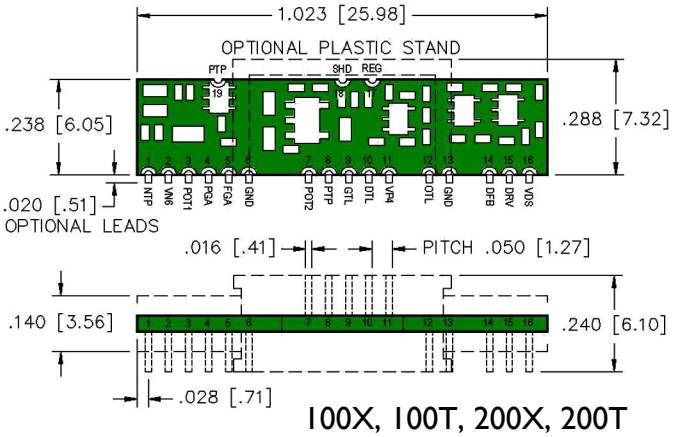
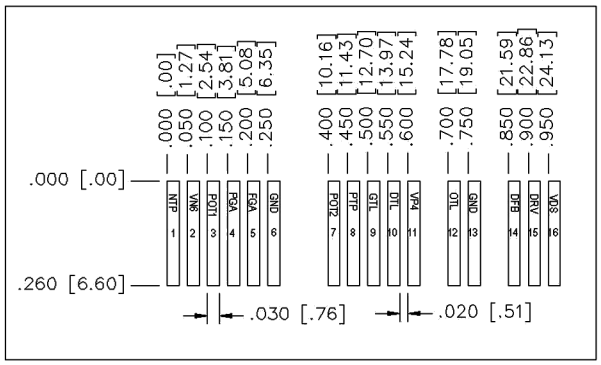
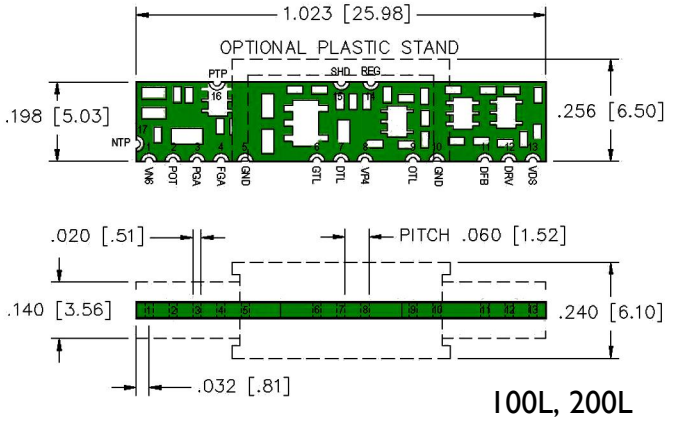
Outline & Land Pattern



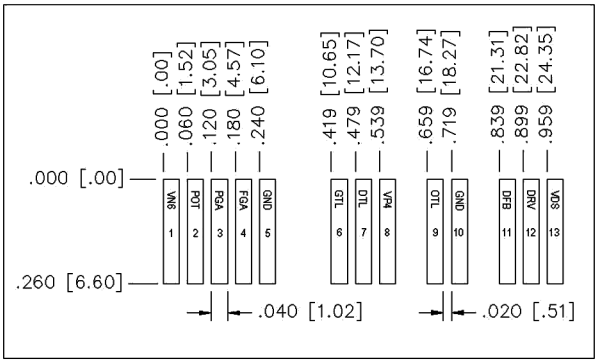
100X, 100T, 200X, 200T



TOLERANCE IS +/−.005" [.13mm]
UNLESS OTHERWISE SPECIFIED



100L, 200L



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Controller I/O Pin Descriptions

WARNING
—Do not connect Outputs together unless specified to do so.
—Do not ground unused Outputs. Leave open.
—Familiarize with the maximum rated voltages and currents.

NTP has –4.3V output from a voltage inverter. Tap with >10KΩ trim-pot to establish (-) input to POT pin of the 100 Series only. Otherwise, leave open.

VN6 input is connected to an optional negative supply of > –6V if gate current boost of 100mA is needed for saturated GaN. Internally, there's 30mA. Leave open otherwise.

POT input receives negative voltage for 100 Series or positive voltage for 200 Series. This unity gain buffer provides negative bias to the transistor gate. Temperature-compensation voltage is added here as well.

PGA output produces a square-wave triggered by TTL to pin GTL. It provides gate bias to GaN at a level set from POT pin and down to V_pinchoff established from either the voltage inverter (-4.3V) or from pin VN6.

FGA output has a fixed gate bias voltage typically used by models with NO gate switching capability. May also be used as auxiliary bias for GaN drivers.

PTP has +5.0V output from a voltage regulator. Tap with >10KΩ trim-pot to establish (+) input to POT pin of the 200 Series only. Otherwise, leave open.

GTL input takes active-low, TTL signal (<4.7V) to control gate switching of the device. It is tied to DTL pin to sequence the gate and drain voltage. This is not used for sub-models. Disconnect from DTL for independent control.

DTL input controls the drain switching end of the transistor. When tied with GTL, the active-low TTL enable switches drain voltage ON and would remain there until gate voltage undergoes a full ON/OFF cycle. Oscillations are mitigated when device is in pinch-off during ramping Vdd up & down.

VP4 input is connected to an optional supply of ≤ +5V. Leave open unless required by sub-models.

OTL output is an active-low TTL drive signal reserved for 300 Series Power CMOS switches. Leave pin open otherwise.

DFB input monitors the presence of drain voltage when the MOS switch is ON. Use if gate switching is desired; otherwise, leave open for sub-models.

DRV output connects to the gate input of MOSFET switch module. Connect to multiple switches with up to 300mA total loads.

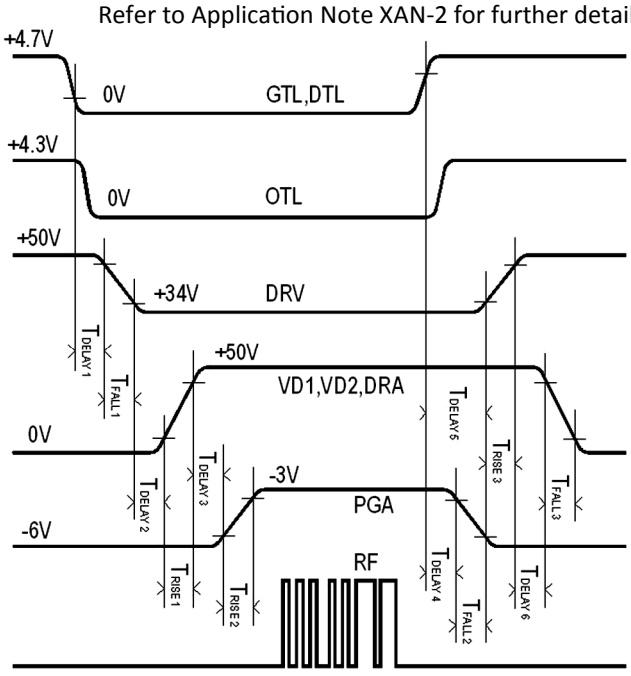
VDS input receives up to +80V from the same supply that powers the GaN.

REG is an auxiliary port of +5.7V from a voltage regulator.

SHD is an auxiliary port for adjusting the gate voltage shutdown threshold. From this node, connect 100KΩ-1MΩ resistor to REG (or PTP) ports for increasing the threshold level, or to GND for decreasing said level.

Typical Timing Diagrams

Refer to Application Note XAN-2 for further details.



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