An Efficient High Speed & Low Power Hybrid Full Adder

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Abstract- In this project, the propose of Hybrid full adder CMOS design is presented. There are various design modules are to implement the hybrid full adder design. Transmission gate logic based Hybrid full adder design is apply in this project by using complementary metal oxide semiconductor (CMOS) logic for low power function. Here general, the full adder performance evaluation is analyzed for 1bit. For high speed applications, the proposed design is used and also it reduces the delay and power than existing design. There are various logics that be use to design a full adder to check the synthesis comparisons through schematic design. In terms of area power and speed the hybrid full adder offers implement and significant when compared with the previous design of full adder. Full adder is mostly used in configuration of cascading, due to the during capability of full adder. Proposed is designed in mentor graphics. These output waveform and simulation results are evaluated in mentor graphics tool.

Keywords- Low power, Hybrid Adder design, power delay product.

I. INTRODUCTION

The adder plays a significant quality in complex arithmetic and computational circuits. For example, multiplier, comparator and parity checker. Here current years, more methodologies have been projected to execute a low power full adder. Fast arithmetic calculation cells include adders and multiplier is the as a rule regularly and generally utilized circuits in very-large-scale integration (VLSI) systems [1-15].
The XOR-XNOR circuits be essential structure block in different circuit's particularly mathematics circuits (adders and multiplier), comparator, parity checker, code converter, error-detecting or error-correcting code and phase detector. Adders are the fundamental structure square of composite arithmetic circuit like addition, duplication, division, exponentiation etc. The circuit interruption is controlled with the quantity of reversal point, the quantity of transistor in run, transistor size (i.e., channel width) and the intra cell wiring capacitance. Circuits estimate relies on the quantity of transistor, their size and on the wiring complexity. Some utilization single logic plan used for entire full adder like alternate use other than single logic design for their execution. Power is one of the imperative possessions, thus the originators attempt to low power as planning a framework. Power dissipation relies on the exchanging movement, node capacitances, and control circuit measure. Through choosing appropriate W/L relation can be limit the power dissipation without diminishing the supply voltage. Various logic designs tend to support one execution perspective to the detriment of previous.
In this paper, projected 1-bit and adjusted 1-bit hybrid full adder is structured. The projected hybrid full adder comprises of XNOR and carry production module. The XNOR module is in charge of the greater part power utilization of the whole adder circuit. For the planned hybrid full adder, six transistor XNOR circuits [6-15]. For development hybrid full adder, four transistor XNOR circuits are utilized. Contrasting and the current adders CMOS, the nature of the developed with changed hybrid full adder explain with the purpose of the plan has the most excellent delay, PDP, total power dissipation and area. Because of the lowest delay, the adder core significantly improves the general execution designed for a huge range of a multi-bit adder. This document is composed as following: II explain about the full adder propose. III explain about the designs of proposed and developed hybrid full adder and the operation of 64 bit ripple carry adder. IV implemented the reproduction results in mentor graphic (130nm), further in V conclusions are represented.

II. FULL ADDER

In full adder circuit a combinational circuit. That completes adding operation with three input bits. In generally have three input bits and two output bits. The input bits are taken as A, B, C. Coming output bits are taken as sum(s) and carry(c) display the important diagram of the full adder circuit and the general Boolean equation for the operation is given below:

Sum= ((A EX-OR B) EX-OR C),
Carry=BC+ BA + CA.

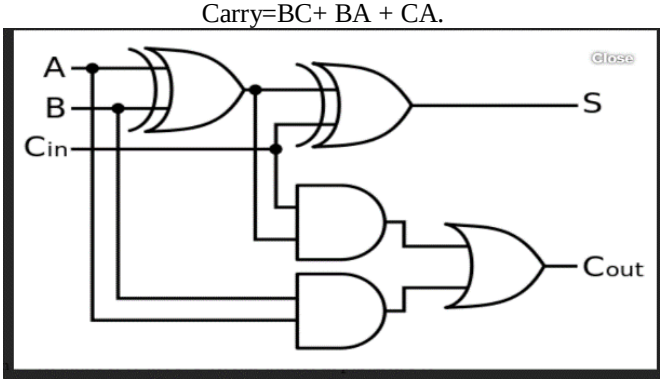

Fig.1: Full Adder Logic Diagram

INPUTS			OUTPUTS	
A	B	C_{in}	SUM	CARRY OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

TABLE.1 FULL ADDER TRUTH TABLE

III. Proposed of Models Adder Circuits:

A. FULL ADDER using 28T

In one-bit straight CMOS full adder unit is shown in fig. One-bit full adder unit have 28transistors. CMOS propose mode be not area capable for multipart gates with great fan-in. Think about have to be occupied while a stationary reason method be particular near understand a reason occupation. A conventional plan of standard inactive CMOS full adder is stand on intended CMOS construction with conventional PMOS and NMOS transistor.

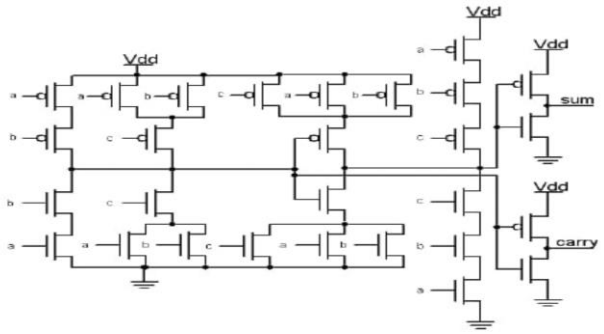

Fig.2: 28T Full Adder

B. FULL ADDER using 14T

To decrease the quantity of uses transistors in the usual full adder, XOR & XNOR circuits. The progress of 14 transistor full adder lead to improved effect intended for hold-up the same as power consumption as evaluate towards before work in the full adder. 14 transistor full adder effort fine among high presentation multiplier by small amount of power dissipation. But adder does not prove expansion in entrance power failure. The 14 transistor adder by 14transistors munches through extensively fewer power during the arrange in command of microwatts also it have high speed. In this unit is designed with use of 4transistor XOR gate. It is important factor of full adder unit along with produces the necessary adding task of adder unit. Here 14transistor full adder unit we utilize twice 4transistor XOR gate. At this point we cover 4transistor XOR gate to enlarge path mass by means of this XOR gate, else during volume of full adder is realize and on the whole outflow is also compact.

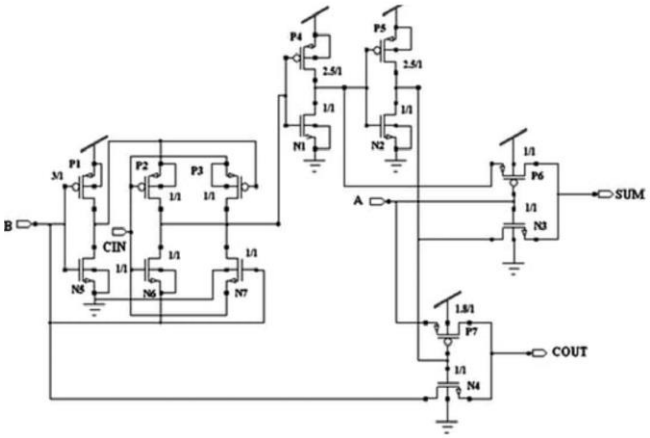

Fig.3: 14T Full Adder.

C. FULL ADDER using 10T

The design of 10Transistor Adder is a 1-bit full adder have 3 variable inputs a, b, c and 2 variable outputs sum S and carry C. The Adder unit is constructed with 5 CMOS inverters with the purpose of shown during Figure. "A" is directly fed to the initial inverter, while in "B" is fed to the subsequent and following inverters. Succeeding inverter PMOS and NMOS of the following inverter are fed to initial inverter intermediate result, though subsequent inverter NMOS and inverter of following one is fed straightforwardly to the input of A. subsequent inverter result is coupled fourth inverter and input variable C is given to the input of inverter fifth. Present VDD power supply linked to the initial inverter only. The proposed model of full adder is set up toward the low power utilization and a lesser amount of power-delay result in pulse reproduction by balance with the extra previous style, the nature of the full adder hybrid circuit explain, in order to explain best power-delay result of carry signal. Owing to the least amount of time holdup carry, the adder part is significantly get better the on the whole presentation for a range of multipath adder. The circuit doesn't contain every straight pathway to position. Appropriate to this development power utilization be able to decreased. In this circuit there have been placed 2 XNOR circuits which are cascade form. In the circuit sum signal has produces and then carry signal is generate all the way through the transmission gate.

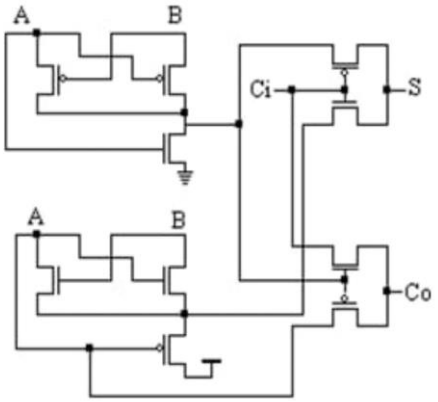

Fig.4: 10T Full Adder

D. FULL ADDER using 8T

The Propose of full adder is support on 3 transistor XOR gates. The 3 transistor XOR gate is power dissipation of to some extent more than that of the 4 transistor XOR gate. 3 transistor XOR gate has greatly take away interruption than 4transistors XOR gate so that has a less power-delay product. The noise boundary of the 3 transistor XOR gate is also improved than the 4 transistor XOR gate. The heart of propose is base going on a adapted description of a CMOS inverter. While the variable B is high reason, the inverter purpose similar to a usual CMOS inverter. So the output A XOR B is the go mutually input A. The voltage deprivation suitable to entry drop is able to be decrease by raise the percentage of W/L CMOS inverter. Evaluate to the before considered 10 transistor full adder, the adder give you an idea about in upgrading in area and power interruption product. The simulation has been done by mentor graphics.

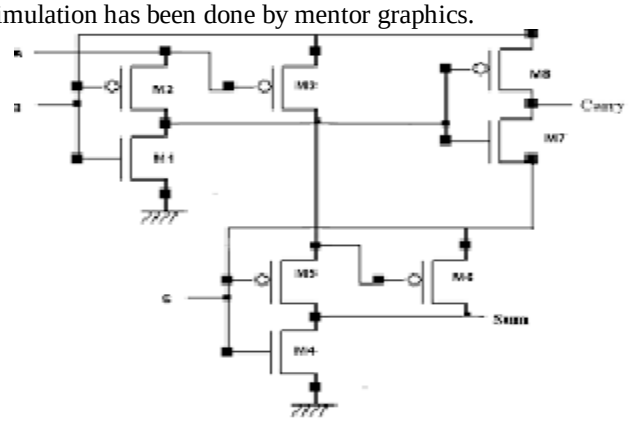

Fig.5: 8 T Full Adder

IV. SIMULATION RESULTS

The following results has obtained for the different full adder circuits in Mentor graphics, below figures shows that simulation, schematics and waveform.

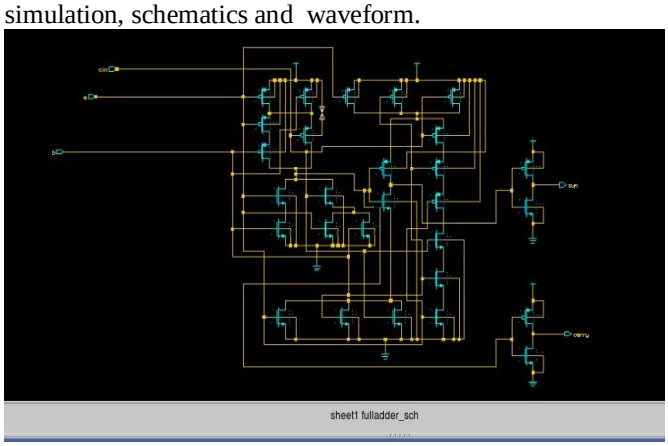

Fig.6: Schematic of 28Transistor Full adder

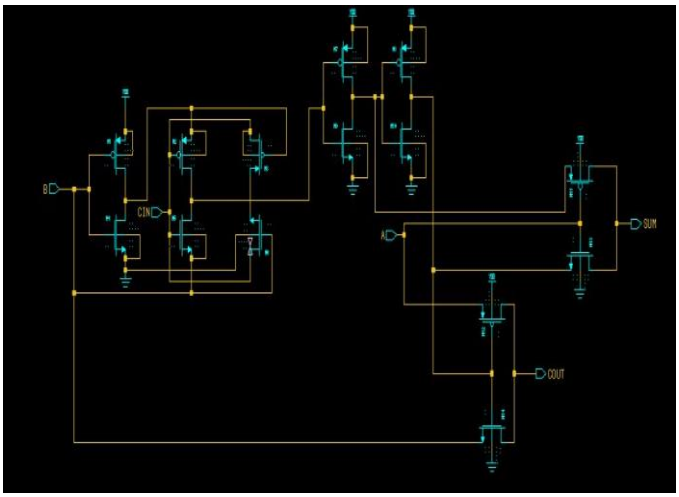

Fig.7: Schematic of 14Transistor Full Adder

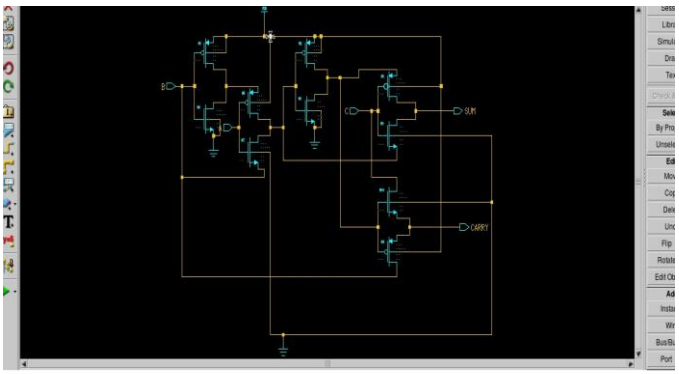

Fig.8: Schematic of 10 Transistor Full Adder

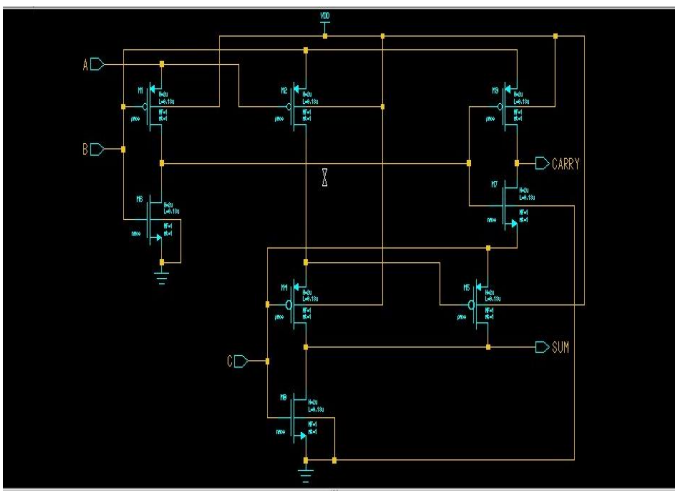

Fig.9: Schematic of 8Transistor Full Adder

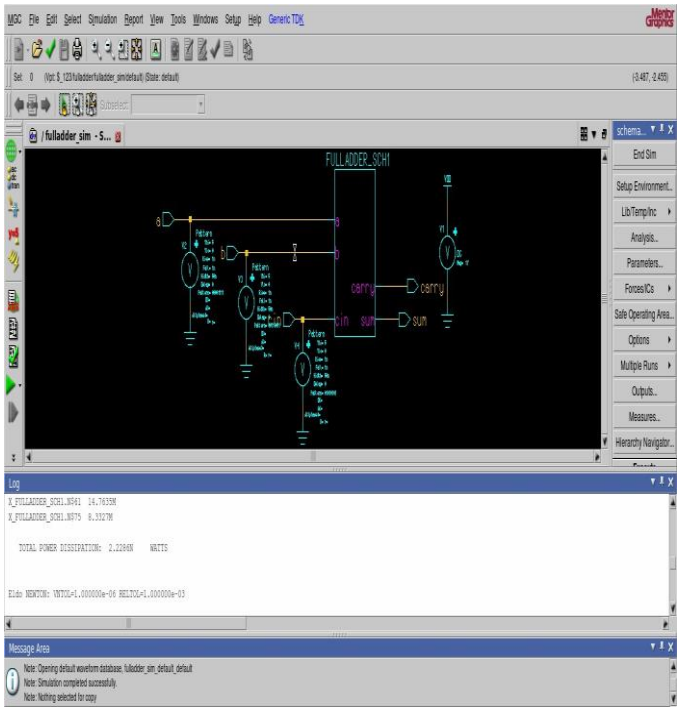

Fig.10: Simulation of 28Transistor Full Adder

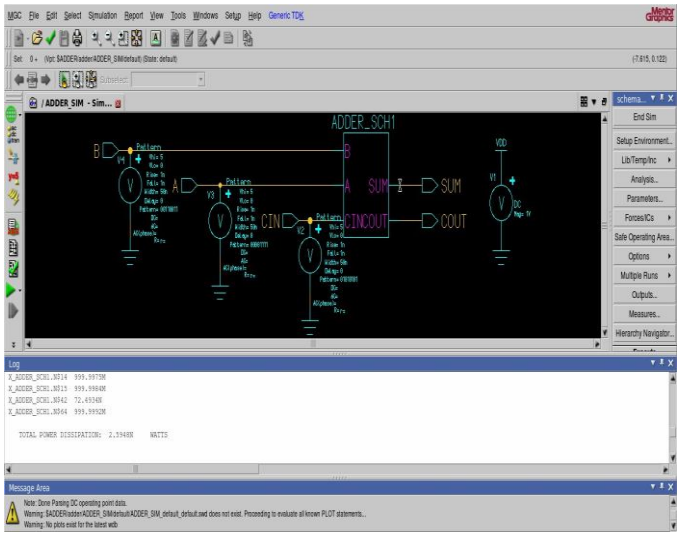

Fig.11: Simulation of 10Transistor Full Adder

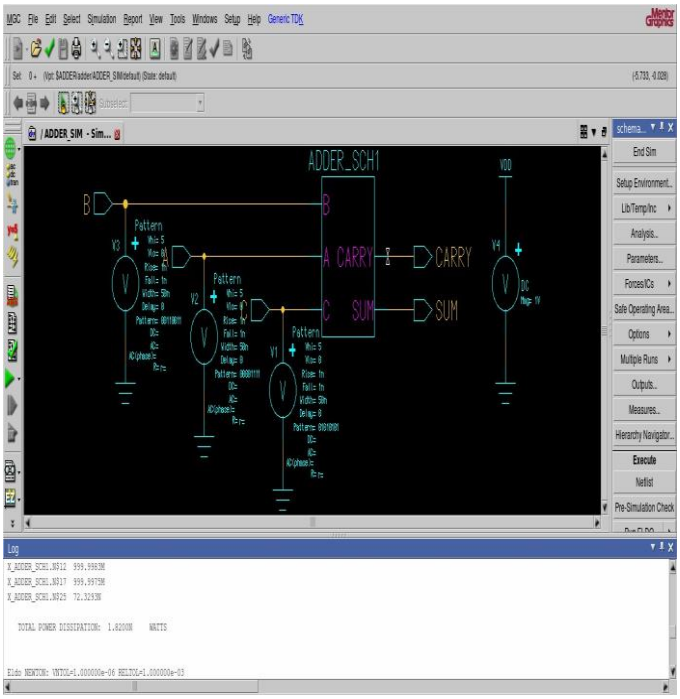

Fig.12: Simulation of 10Transistor Full Adder

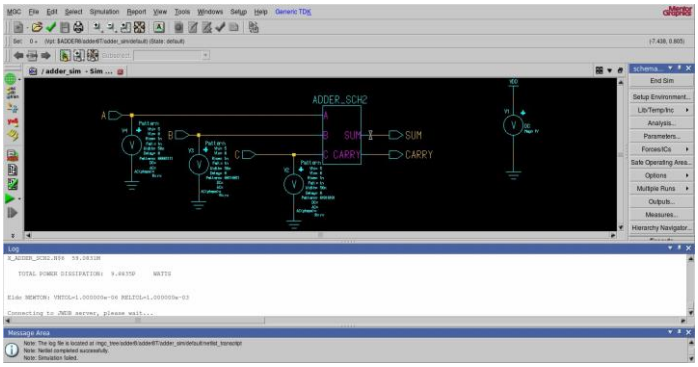

Fig.13: Simulation of 8Transistor Full Adder

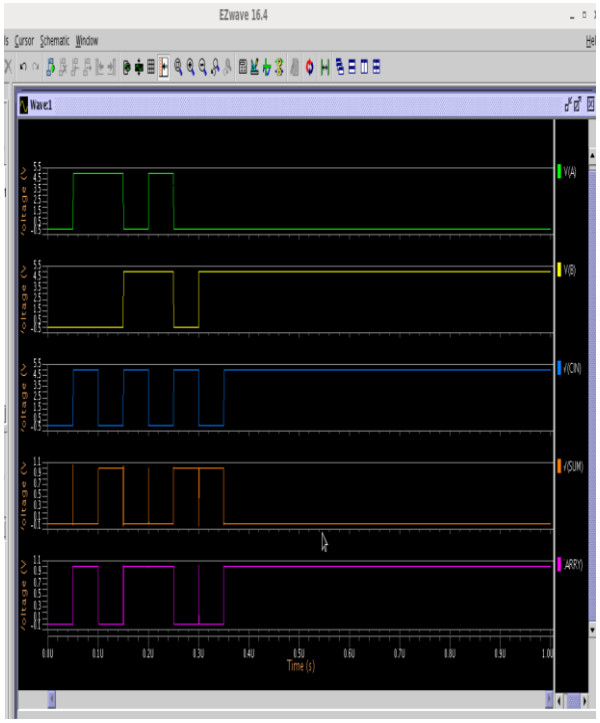

Fig.14: Waveform of Full Adder

V. BAR GRAPH

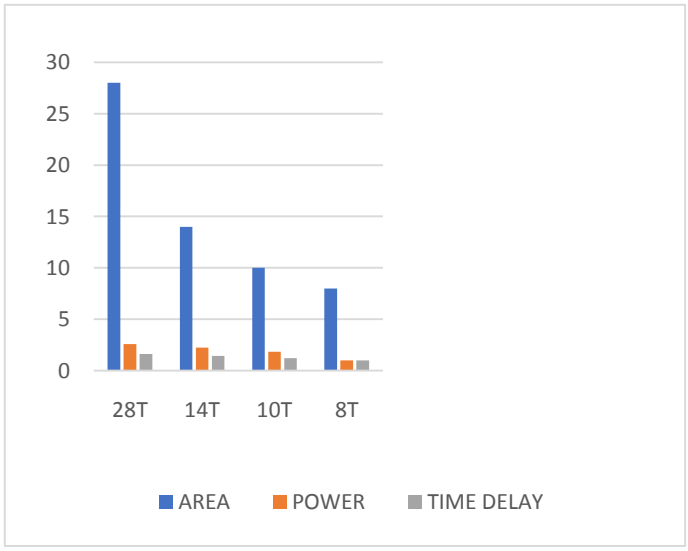

Fig.14: Comparison of different full adders Power in nano watts Time in seconds

VI. CONCLUSION

The proposed 8 Transistor full adder circuit consumes a very power and area by using mentor graphics tool. Mainly this adder can be used in DSP digital circuits where the speed of operation and power consumption required is needed. Outcome explains that the planned devise has high presentation and most excellent PDP in similarity with several pervious full adder designs. As a result this new intend is establish suitable at low voltages and has better output. It is also confirmed during simulation output that proposed design perform well under the projected in supply voltage and temperature.

VII. REFERENCES

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