An Optimized XOR Circuit using CNTFET Technology

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Abstract- In this paper, a varied range of XOR circuits are designed in which 6T XOR is proposed using CNTFET Technology are designed using MOSFET in 32nm Technology length. Then, they are simulated using HSPICE and the performance parameters of adders such as average power and delay are determined. The proposed circuit is compared with 12T CMOS XOR circuit which is conventional used and compared with CNTFET counterpart of the XOR gate. Simulation results show that the proposed XOR gate is better in performance.

Keywords- CNTFET, Nano tubes, XOR, 32nm, 6T XOR

I. INTRODUCTION

As CMOS keeps on scaling further into the nanoscale, different gadget non-idealities cause the I-V qualities to be considerably not quite the same as all around tempered MOSFETs. For instance, the source/deplete arrangement obstruction is presently a noteworthy segment of the aggregate on-opposition. Proposition of metal reached (Schottky) source/drain UTB SOI FET likewise change the I-V qualities fundamentally. Novel non-Si gadgets, for example, the carbon nanotube FETs (CNTFETs) work with totally unique gadget material science with semi ballistic transport in the station and Schottky obstructions at the source/deplete contacts.

As one of the promising new gadgets, CNTFET keep away from the greater part of the key restrictions for customary silicon gadgets. All the carbon molecules in CNT are attached to each other with sp2 hybridization and there is no dangling bond which empowers the coordination with high-k dielectric materials. So we attempt to fabricate some advanced circuit utilizing CNTFET and advance them.

II. PROPOSED XOR DESIGN USING CNTFET

In hardware, a XOR is a circuit that duplicates two stable states and is utilized as a fundamental piece in an Arithmetic and Logic Unit. It is imperative to enhance parameters in a XOR as it most ordinarily utilized piece of rationale unit. In our proposed strategy, we supplant regular MOSFETs with CNTFETs, and a comparitive examination of measurements like Average Power Consumption, Delay, PDP and Power Dissipation Voltage Source is computed.It is found that in terms of all performance metrics mentioned, the 6T CNTFET circuit is the best configuration circuit for XOR gates.

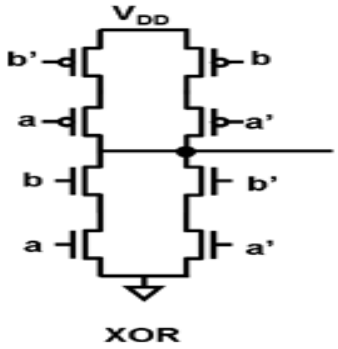

Fig.1: 12T CMOS XOR Gate

The proposed design of 6T XOR is given in Figure 4 and in Figure 3 Conventionally used 12T XOR gate is shown. In 6T XOR, basically two inverters and one pass transistor forms the logic of XOR gate. As in XOR gate, when both inputs are different output is 1 and when both inputs are same output is 0. This can be easily verified on the 6T XOR gate.

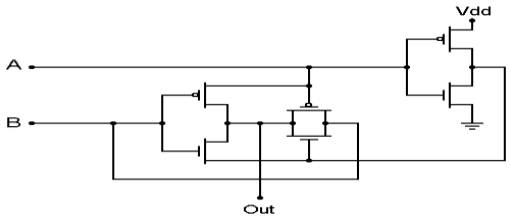

Fig.2: Circuit for 6T XOR usingMOSFET

While using CNTFET, we have to consider several factors like no. of tubes, pitch, width efeective, etc, the schematic is similar to the MOSFET one by changing the device to CNTFET as shown in Figure 5 and Figure 6. In Figure 5, circuit of conventional XOR gate 12T using CNTFET is shown. And in Figure 6, circuit of proposed CNTFET based 6T XOR gate is shown.

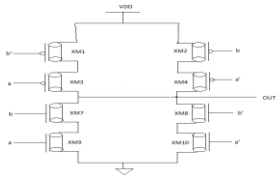

Fig.3: Circuit for 12T XOR usingCNTFET

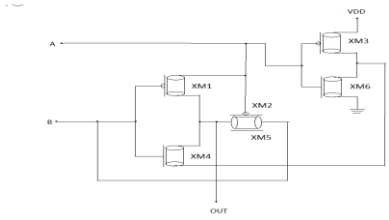

Fig.4: Proposed Circuit for 6T XOR usingCNTFET

Our proposed method for making a XOR functianlity utilizing CNFET working precisely and the outcomes are exhibited out in this paper. For the reenactment we utilize the stanford CNFET Hspice demonstrate for Simulation at 32nm innovation. The proposed technique improves the transistor circuit Average Power Consumption, Delay, PDP and Power Dissipation Voltage Source Parameters.

III. SIMULATION RESULTS

This has been proficient by proposing another enhancement strategy. To demonstrate the adequacy of the proposed gate level plan technique, recreation has been performed utilizing HSPICE with the Stanford CNTFET library. [13]Results have shown that the proposed outline approach is both successful and common. To outline a CNTFET circuit, numerous parameters must be considered, among them the distance across at certain chirality, pitch. The parameters, for example, limit voltage, gate capacitance, deplete present, ideal fan-out factor can be controlled by pitch, chirality and the quantity of carbon nano tubes. Table 1 introduces the measurements correlation between CNTFET based XOR and MOSFET based XOR.

Figure 7 and Figure 8 shows to Average Power Comparison in XOR 12T and 6T. It obviously demonstrates that CNTFET XOR in 32nm innovation is a superior choice with 6T. In table 1 all simulation results are presented,

Table 1: Simulation Results

	12T XOR MosFET	12T XOR CNTFET
Average Power (12T)	6.50E-07	3.57E-07
Delay (12T)	4.76E-08	4.79E-08
PDP	3.09E-14	1.71E-14
Power Dissipation Voltage Source	1.72E-07	6.11E-10
	6T XOR MosFET	6T XOR CNTFET(proposed)
Average Power (6T)	1.95E-06	7.26E-08
Delay (6T)	8.96E-11	8.81E-11
PDP	1.75E-16	6.40E-18
Power Dissipation Voltage Source	4.62E-05	1.65E-10

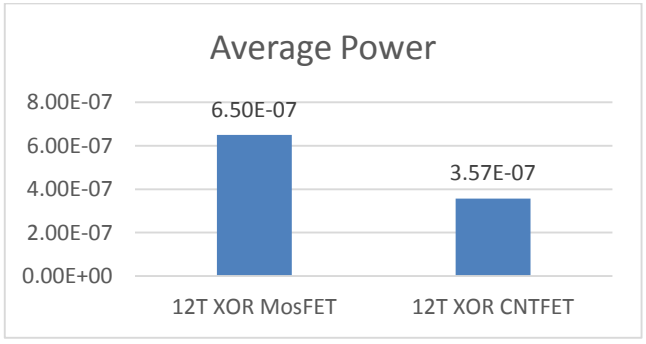

Fig.5: Average Power in XOR 12T

In Figure 9 Delay comparison of 6T XOR is represented. Table 1 gives a tabular representation of the results.

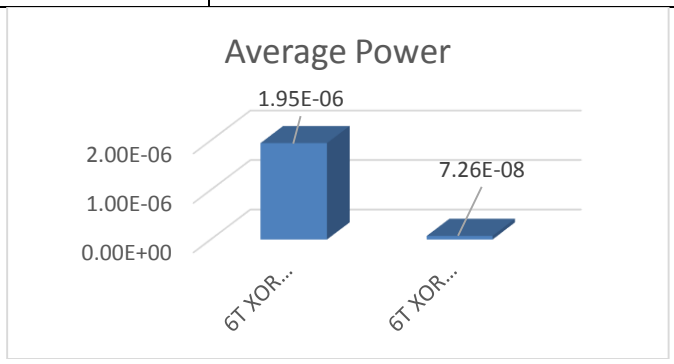

Fig.6: Average Power in XOR 6T

It shows when we use CNTFET replacements the Delay, Average Power Consumption, PDP and Power Dissipation for Voltage a significant improvement in all is obtained in XOR 6T and XOR 12T circuits.

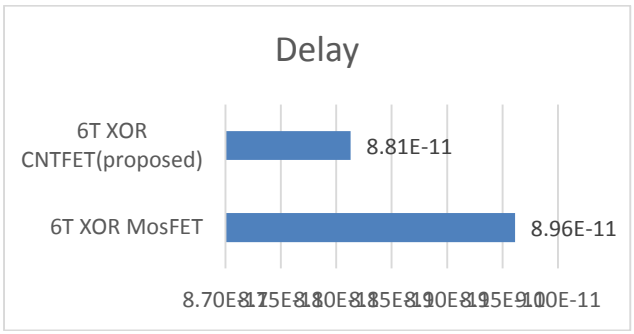

Fig.7: Delay in XOR 6T

Figure 10 and Figure 12 chart shows the improvement in Power Dissipation voltage source for 6T and 12T XOR gate when compared between MOSFET and CNTFET circuits. It shows that CNTFET show better performance.

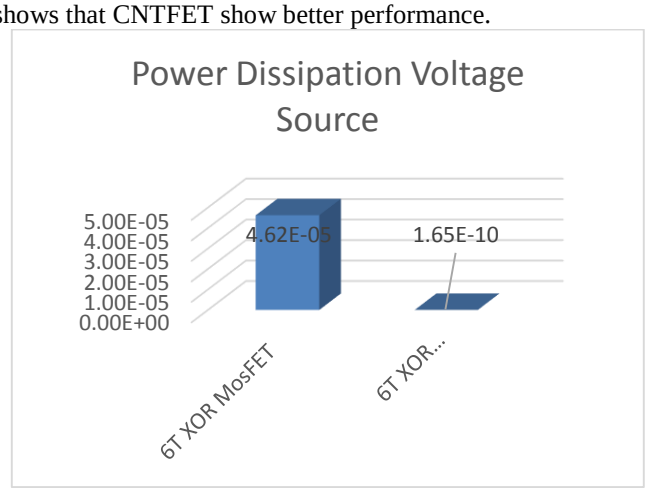

Fig.8: Power Dissipation Voltage Source in XOR 6T

Figure 11 and Figure 13 are charts which represent that PDP is improved when using CNTFET and comparing to MOSFET based XOR in 6T and 12T modes.

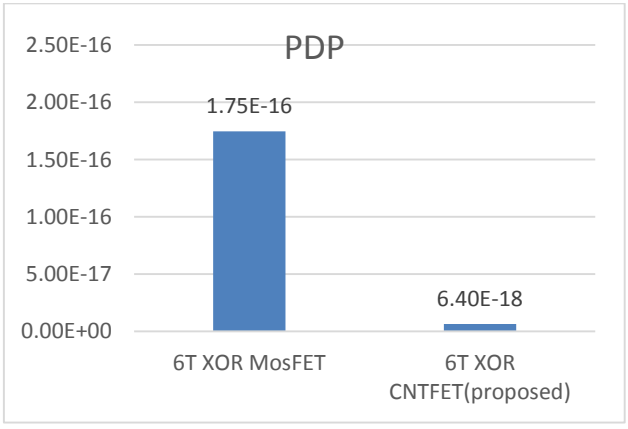

Fig.9: PDP in XOR 6T

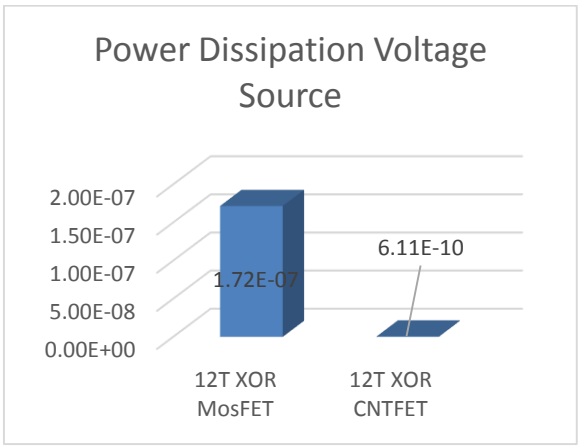

Fig.10: Power Dissipation Voltage Source in XOR 12T

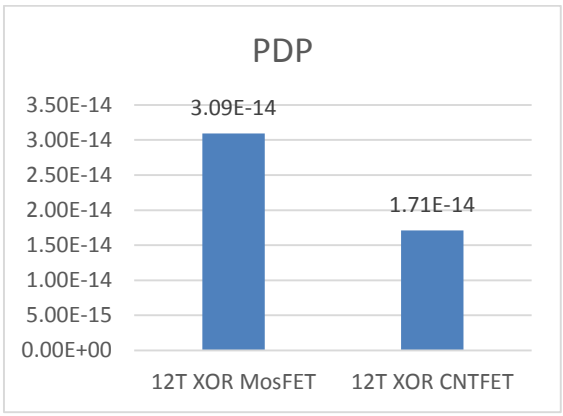

Fig.11: PDP in XOR 12T

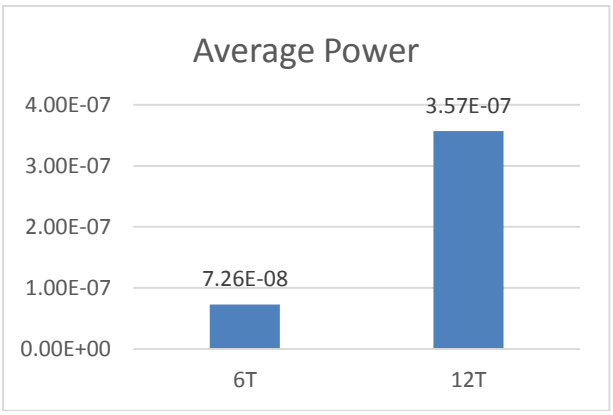

Fig.12: Average Power Consumption in 6T and 12T XOR

Figure 14 and Figure 15 show significant improvement in charts for comparison between 6T XOR CNTFET and 12T XOR CNTFET with respect to Average Power Consumption and Delay. Hence this proves that 6T shows lower power

consumption and higher speed providing the same logic efficiently.

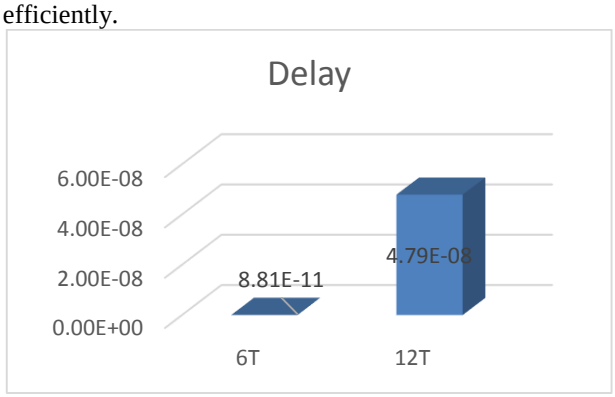

Fig.13: Delay in 6T and 12T XOR

Figure 16 and Figure 17 below show the comparison of PDP and Power Dissipation Voltage source in 6T and 12T CNTFET XOR.

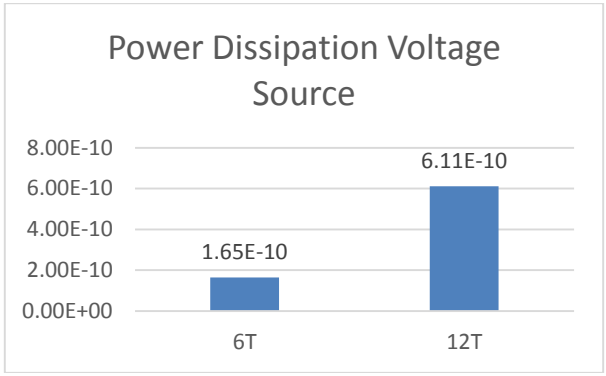

Fig.14: Power Dissipation Voltage Source in XOR 6T and XOR 12T

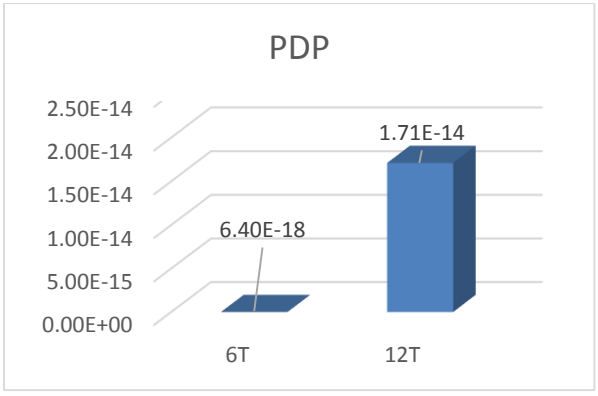

Fig.15: PDP in XOR 6T and 12T

Above results show that CNTFET is the device which can be used to replace MOS type circuits at lower scaled technologies. The table 2 below gives the parameters used in the development of codes in HSPICE software for CNTFET.

Table 2: Parameters for CNTFET Model

Lss	32nm
Pitch	20nm
Length Channel	32nm
No. of Tubes	3
Efo	0.6eV
Kox	12

IV. CONCLUSION

Simulation results show that 6T CNTFET is better in case of XOR gates as Average Power is reduced by 79% and Delay is also reduced by 99.8%. Also significant improvement in the PDP and Power Dissipation Voltage Source which is improved by 99.9% and 72.9 % respectively when compared to 12TXOR gate. The Carbon Nanotube Field Effect Transistor (CNTFET) is a standout amongst the most encouraging gadgets among rising advancements to broaden as well as supplement the conventional Si MOSFET. As the qualities of a CNTFET is not the same as traditional mass CMOS, new plan technique must be built up. As request of new outline technique, this task break down the qualities of CNFET, CNT interconnect advances and propose new strategies to configuration circuits, for example, computerized, memory and I/O circuit. This has been proficient by proposing another streamlining strategy. To demonstrate the viability of the proposed entryway level plan technique, reproduction has been performed utilizing HSPICE with the Stanford CNTFET library. Results have exhibited that the proposed outline system is both successful and functional. In this exploration work a low power XOR has been outline at 32nm innovation utilizing Stanford CNTFET demonstrate the prime spotlight was on procedures which can be utilized for lessening the spillage power dissemination. Postponement is another critical execution metric of a VLSI plan and future work will develop general improvement of the XOR as far as accomplishing low spillage power with fast of task.

V. REFERENCES

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