Static Power Reduction using Variation-Tolerant and Reconfigurable Multi-Mode Power Switches

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Abstract - There are many important applications, such as math function evaluation, digital signal processing, and built in self-test, whose implementations can be faster and simpler if we can have large on-chip "tables" stored as read-only memories (ROMs). We show that conventional de facto standard 6T and 8T static random access memory (SRAM) bit cells can embed ROM data without area overhead or performance degradation on the bit cells. Just by adding an extra word line (WL) and connecting the WL to selected access transistor of the bit cell (based on whether a 0 or 1 is to be stored as ROM data in that location), the bit cell can work both in the SRAM mode and in the ROM mode. In the proposed ROM-embedded SRAM, during SRAM operations, ROM data is not available. To retrieve the ROM data, special write steps associated with proper via connections load ROM data into the SRAM array. The ROM data is read by conventional load instruction with unique virtual address space assigned to the data. This allows the ROM-embedded cache (R-cache) to bypass tag arrays and translation look-aside buffers, leading to fast ROM operations. We show example applications to illustrate how the R-cache can lead to low-cost logic testing and faster evaluation of mathematical functions.

Keywords - Read-Only Memory, SRAM,

I. INTRODUCTION

In this paper, we present the ROM-embedded cache (R-cache) architecture, where a ROM in hardware is embedded into conventional SRAM, with corresponding architectural supports. As we know that a storage cell can work both as a ROM and an SRAM bit, based on the operation requirement. During normal operation, the cache operates in the usual way, and the ROM data is not available. However, when the ROM data needs to be retrieved from a certain section of the cache, the SRAM data is stored temporarily in a buffer. Once the ROM data is retrieved, the SRAM data is transferred back to the corresponding location in the cache. The proposed SRAM (called the ROM-embedded SRAM or R-SRAM) does not incur any area penalty on the bit cells, nor does it degrade the performance (the detailed layout of the bit cell is shown later). Since the SRAM also works as the ROM, there is no need to access external memory to read useful data. We modified two de facto standard thin-cell layouts of the 6T SRAM and 8T SRAM bit-cell layout [6]–[8] to the corresponding thin-cell layouts of 6T R-SRAM and 8T R-SRAM bit cells, respectively. The new layout requires one additional metal line [no area penalty on the bit cell; but 2% area overhead and less than 1% power overhead from an additional wordline (WL) driver for the 6T R-SRAM. Due to increased bit-line capacitance and resistance, in [10], multiple supply power rails are selectively connected to SRAM bit cells to determine the ROM data. Additional transistors are added to the bit cells for the same purpose in [11] and [12]. All the above works call for larger area and/or performance penalty in a significant way. On the other hand, the proposed R-cache is able to maintain the bitcell area and performance of the conventional SRAM design.

II. LITERATURE REVIEW

Author S.Satyanand Nalam, and Benton H. Calhoun proposed a 5-transistor (5T) bitcell that uses sizing asymmetry to improve read stability and to provide an efficient knob for trading off the aforementioned metrics. The 5T bitcell width can be reduced by 28% as compare to 6T bitcell, and also compares the read performance and power of a 5T with a pseudo-differential sensing scheme that is 6T. The main drawbackof the 5T bitcell is an inferior write margin due to the difficulty in writing a '1'.

Saibal Mukhopadhyay, Rahul M. Rao, Jae-Joon Kim and Ching-Te Chuang, proposed a transient negative bit –line voltage technique to improve write ability of SRAM cell. The Capacitive coupling is used to generate a transient negative voltage at the low-going bit-line during Write operation without using any on-chip or off-chip negative voltage source.

Leland Chang, Robert K. Montoye, Yutaka Nakamura, Kevin A. Batson, Richard J. Eickemeyer and Robert H. Dennard proposed a An eight-transistor (8T) cell is proposed to improve variability tolerance and low-voltage operation in high-speed SRAM caches. The main advantage of these operation is that there is no need for secondary or dynamic power supplies and enable low-voltage operation. The 8T cell also provides a simple solution for SRAM stability and write ability that can be achieved without significant are a penalty.

Tyler L. Brandon, Duncan G. Elliott proposed a ROM cell architectures are proposed that have roughly 20% greater storage density in the cell array compared to that of a conventional ROM and also a new SRAM-ROM architecture is presented that capitalizes on these techniques to add ROM capability to a conventional SRAM cell with no additional transistors in the memory cell. The main drawback of these techniques is that as SRAM-ROM requires extra column decoding and has increased BL capacitance, resulting in slower access time and greater power consumption.

III. METHODOLOGY

The most commonly used SRAM type is the 6T SRAM which offers better electrical performances from all aspects (speed, noise immunity, standby current)Fig. 1 describes a conventional 6T SRAM bit cell. As the thin-cell layout topology is a de facto standard in the industry because of its compact area, better tolerance to variability and high performance. Also, the contact forWL signals is shared by two neighboring SRAM bit cells. For each row, there is one metal line of WL. Hence, gate signals of all the access transistors in the same row are turned on and off simultaneously.

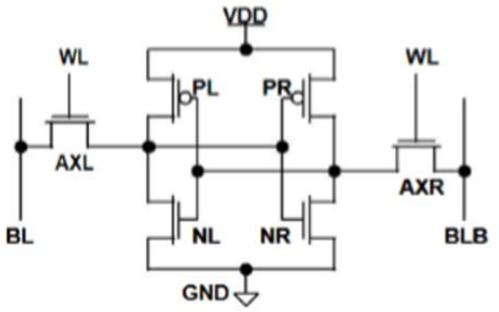

Figure 1: Conventional 6T SRAM Schematic design.

IV. CONCLUSION

We proposed a new R-cache architecture. The R-cache does not incur area/performance penalty on the SRAM bit cells. The R-cache for the 6T configuration uses one additional WL, and the SRAM access transistors are connected to one of the two WLs depending on the data to be stored in the ROM. For the 8T R-SRAM configuration, the R-cache connects the read transistor to either ground orRCON, depending on the data to be stored in the ROM. We analyzed both SRAM and ROM stability in scaled technologies and presented techniques to improve the yield. We also considered possible applications of the R-cache. To improve evaluation time/accuracy of complex math functions, the R-cache can store large tables on-chip (while still being able to perform standard SRAM operations). The size of the tables is limited only by the size of on-chip caches. The proposed methodology improved evaluation latency for double-precision elementary mathematical functions by ∼30%compared to conventional evaluation techniques. We also presented a new deterministic logic BIST methodology that consists of test data compression logic and the R-cache, which can store and deliver the test data without the support of external ATEs.

V. REFERENCES

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