S.NO	TITLE	YEAR	ABSTRACT
SPVL-01	Approximate Radix-8 Booth Multipliers for Low-Power and High-Performance Operation	2016	The Booth multiplier has been widely used for high performance signed multiplication by encoding and thereby reducing the number of partial products. A multiplier using the radix-4 (or modified Booth) algorithm is very efficient due to the ease of partial product generation, whereas the radix-8 Booth multiplier is slow due to the complexity of generating the odd multiples of the Multiplicand. In this paper, this issue is alleviated by the application of approximate designs. An approximate 2-bit adder is deliberately designed for calculating the sum of 1_ and 2_ of a binary number. This adder requires a small area, a low power and a short critical path delay. Subsequently, the 2-bit adder is employed to implement the less significant section of a recoding adder for generating the triple multiplicand with no carry propagation. In the pursuit of a trade-off between accuracy and power consumption, two signed 16_16 bit approximate radix-8 Booth multipliers are designed using the approximate recoding adder with and without the truncation of a number of less significant bits in the partial products. The proposed approximate multipliers are faster and more power efficient than the accurate Booth multiplier; moreover, the multiplier with 15-bit truncation achieves the best overall performance in terms of hardware and accuracy when compared to other approximate Booth multiplier designs. Finally, the approximate multipliers are applied to the design of a low-pass FIR filter and they show better performance than other approximate Booth multipliers.
SPVL-02	An Efficient Hardware Implementation of Canny Edge Detection Algorithm	2016	The edge detection is one of the key techniques in most image processing applications. The canny edge detection is Proven to be able to significantly outperform existing edge detection techniques due to its

			superior performance. Unfortunately, the implementation of the systems in real-time is computationally complex, high hardware cost with increased latency. The proposed canny edge detection algorithm uses approximation methods to replace the complex operations; the pipelining is employed to reduce the latency. Finally, this algorithm is implemented on Xilinx Virtex-5 FPGA. When compared with the previous hardware architecture for canny edge detection, the proposed architecture requires fewer hardware costs and takes 1ms to detect the edges of 512x512 image.
SPVL-03	Built-in Self-Heating Thermal Testing of FPGAs	2016	Field Programmable Gate Arrays (FPGAs) are designed and fabricated using the most advanced CMOS technology nodes to meet performance and power demands. This makes them Susceptible to many manufacturing and reliability challenges. Increasing chip temperature is a major reliability concern since various failure mechanisms are accelerated at high chip temperature, which require thermal-aware testing to detect them. External devices like thermal chambers are usually used to heat up the chip to a desired temperature in order to apply the test. However, there are many limitations for these external devices, which make the thermal-aware testing of the FPGA a challenging process. In this paper, thermal-aware testing of FPGAs using built-in self-heating is presented, in which the internal resources of FPGA are used to build controlled self-heating elements (SHEs). These controlled SHEs are distributed across the FPGA and integrated with the test scheme to generate the required temperature profile for testing, and thus no external devices for heating up the FPGA are needed. We present two different categories of SHEs integration techniques for different testing purposes. The first one is for built-in self-test (BIST), and the second one is for application-dependent testing. The techniques are applied on representative test

			cases. The experimental results show that a wide range of maximum chip temperatures can be Achieved (from 50_C up to 125_C on Virtex-5 FPGA) with a high accuracy (_ 1_C).
SPVL-04	A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications	2016	Transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike direct form configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on a detailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. A generalized block formulation is presented for transpose form FIR filter. We have derived a general multiplier-based architecture for the proposed transpose form block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less area delay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, The block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. Application specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involves 42% less ADP and 40% less EPS than the best available FIR filter Structure proposed for reconfigurable applications. For the same filter length and the same block size, the proposed structure

			involves 13% less ADP and 12.8% less EPS than that of the existing direct-form blocks FIR structure.
SPVL-05	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels	2016	In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption Compared with the conventional one. The speed enhancement is achieved by applying concatenation and incrimination schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skip logic. The structure may be realized with both fixed stage size and variable stage size styles, wherein the latter further improves the speed and energy parameters of the adder. Finally, a hybrid variable latency extension of the proposed structure, which lowers the power consumption without considerably impacting the speed, is presented. This extension utilizes a modified parallel structure for increasing the slack time, and hence, enabling further voltage reduction. The proposed structures are assessed by comparing their speed, power, and energy parameters with those of other adders using a 45-nm static CMOS technology for a wide range of supply voltages. The results that are obtained using HSPICE simulations reveal, on average, 44% and 38% improvements in the delay and energy, respectively, compared with those of the Conv-CSKA. In addition, the power–delay product was the lowest among the structures considered in this paper, while its energy–delay product was almost the same as that of the Kogge–Stone parallel prefix adder with considerably smaller area and power consumption. Simulations on the proposed hybrid variable latency CSKA reveal reduction in the power consumption compared with the latest works in this field while having a reasonably high speed.

SPVL-06	Implementation of a PID control PWM Module on Altera DE0 Kit Using FPGA	2016	The main aim of this paper is to design PID control PWM module using field programmable gate array (FPGA) technology. FPGA based realization offers high speed, complex functionality, consume less power, and provides parallel processing. In this paper, we have implemented PID control PWM module on programmable logic design software Quartus II and verified on DE0 Nano Board (Cyclone IV FPGA family of Company Altera). Signal Tap II analyzer and RTL viewer are used for analyzing and debugging the design. For Proper timing constraint and clock arrangement, Time Quest analyzer is used. The simulation and hardware results shows that implementation with FPGA has some advantages such as flexible design, high Reliability and high speed.
SPVL-07	Distributed Sensor Network-on-Chip for Performance Optimization of Soft-Error-Tolerant Multiprocessor System-on-Chip	2016	As transistor density continues to increase with the advent of nanotechnology, reliability issues raised by more frequently appeared soft errors are becoming even more critical to the next-generation multiprocessor systems. In this paper, we present a systematic approach to address the soft-error problem in multiprocessor system-on-chip with the consideration of system performance optimization. To guarantee the system correctness, a hardware–software collaborated approach is proposed to protect the processors from soft errors. Tiny hardware sensors are embedded in the processor cores to detect the soft errors, and the software-based rollback scheduling mechanisms are applied for error recovery. The protection costs on hardware duplication and software redundancy are effectively reduced. To optimize the system performance, a distributed control system is built on top of the on-chip communication network and collaboratively manages the entire chip for application execution. With the cluster-based task migration techniques, an efficient runtime task remapping and rescheduling algorithm is proposed to further

			mitigate the overheads induced by soft-error protection and to minimize the total performance degradation. The distributed control strategy makes the system more adaptable and flexible to the development of the next-generation hardware and software with larger scales. Extensive performance evaluations using System C-based cycle accurate simulations on a set of real-world applications show that our approach has on average 49% performance improvement and 79.6% energy consumption reduction compared with the related state-of-the-art techniques, and hardware synthesis results show that our approach only introduces 2.9% chip area overheads.
SPVL-08	A Low-cost and Modular Receiver for MIMO SDR	2016	This article outlines the development of a low-cost receiver for Software Defined Radio (SDR) to receive a data burst on an intermediate frequency of 113 MHz This data will have to be sampled and demodulated. Constellations are plotted in real time and Bit Error Rate (BER) is also continuously determined. The original data is received on 2.45 GHz and transformed to an intermediate frequency by the receiver front-end. The received Signal is then buffered, filtered, amplified and demodulated. This is all done in hardware. After this, the microcontroller takes over to process the signal, showing the data as a constellation diagram on the display.
SPVL-09	An FPGA-Based Cloud System for Massive ECG Data Analysis	2016	In this brief, we propose a stand-alone SOPC (System on a Programmable Chip) based cloud system to accelerate massive ECG data analysis. The proposed system tightly couples network IO handling hardware to data processing pipelines in a single FPGA, offloading both networking operations and ECG data analysis. In this system, we first propose a massive session's optimized TCP/IP hardware stack using macro pipeline architecture to accelerate network packet processing. Second, we propose a streaming architecture to accelerate ECG signal processing, including QRS detection, feature

			extraction and classification. We verify our design on XC6VLX550T FPGA using real ECG data. Compared to commercial servers, our system shows up to 38X improvement in performance and 142X improvement in energy efficiency
SPVL-10	VLSI Realization of a Secure Cryptosystem for Image Encryption and Decryption	2016	Chaotic maps have been widely used in data encryption. However, a number of chaos-based algorithms have been shown to be insecure. The application of BB equation for encryption is reported in a recent article. In this paper, new algorithms based on chaos and BB equation are reported for image encryption and decryption. The algorithms are illustrated through an example. For practical use, VLSI architectures of the proposed algorithms are designed and realized using Xilinx ISE VLSI software for hardware implementation. Further, the hardware complexity of the proposed algorithms is compared with the algorithm reported in