A Low-Cost Programmable Digital Sawtooth Wave Generator

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ABSTRACT- Direct digital synthesis based sawtooth wave generators have a complex structure and therefore are not found suitable for various low cost applications**.** In various laboratories for the environment of under graduate students user friendly instruments are desirable. In this paper a very simple and low-cost ramp generator with programmable slope, using off-the-shelf components, is presented. The circuit was tested using software simulation using Electronics Workbench. The results are also presented.

KEY WORDS: *Sawtooth wave, DDS, Counter, A/D converter, Multiplexer, Frequency divider*

I. INTRODUCTION

Sawtooth wave generators find application in many electronic instrumentation systems. Both analog and digital technologies are used to generate sawtooth waveforms [1-4]. Analog based circuits are simple to design but are vulnerable to noise and have poor linearity. On the other hand digitally implemented circuits offer an advantage of good linearity and immunity to noise. Therefore different systems are preferred where accuracy is of prime importance. Also, due to the advent in VLSI technology, the size and the cost of ICs have drastically got reduced thus making the electronic systems cost effective in most of the cases. Digitally tuned sawtooth wave generators can offer flexibility when ramps with different slopes are desired. Direct digital synthesis based sawtooth generator remains the first choice for a designer when different highly linear slopes are required. But the main disadvantages of such circuits are complexity of algorithms [5] and high cost because of engineering charges, thus making it not suitable for many low cost applications. A simple circuit is proposed in this paper for such applications. The paper is organised as follows: In section II, background of digital sawtooth generators is discussed. Section III discusses the proposed programmable sawtooth generator. Finally, in Sections IV and V, results and conclusion are presented respectivey.

II. BACKGROUND

Fig. 1 shows the basic structure for generating sawtooth waves. The digital to analog converter (DAC) is driven by an up-counter which starts from all zero state and keeps on incrementing linearly one by one for every clock pulse till it reaches to all one state. Each time a pulse is inserted in to the counter, the output of

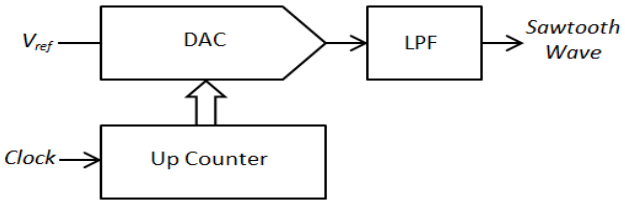
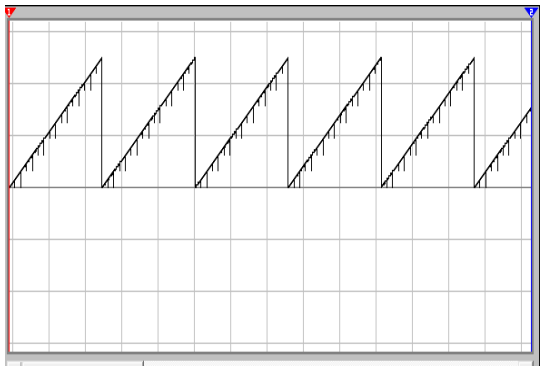
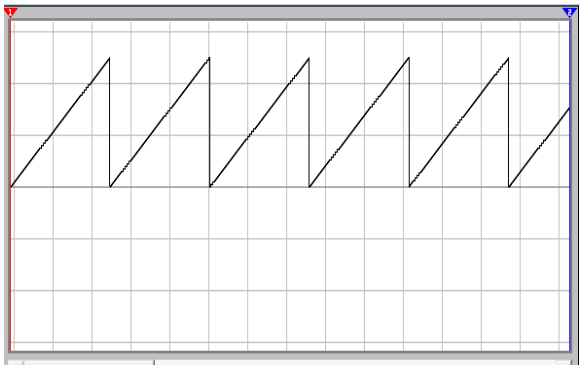


Fig 1: Basic digital saw tooth generator



(a)



(b)

Fig 2: Waveform generated at the output of (a) DAC and (b) Filter

the DAC gets increased till it reaches the maximum full scale value of the DAC. Upon the occurrence of $(2^n + 1)^{th}$

clock pulse the counter comes in all zero state again and hence the DAC output becomes zero as shown in Fig. 2(a). The output of the DAC comprises of harmonics which can be eliminated by a low pass filter (LPF) as shown in Fig 2(b). As depicted from the figure the slope of the ramp is fixed and there is no way of changing it in its basic structure.

The direct digital synthesis (DDS) based generator on the other hand offers flexibility of programmability of ramp slopes by control signals as shown in Fig. 3. It uses a ROM in place of the up counter for storing look-up table (LUT) addressed by the phase accumulator. The look up table stores the pattern of the wave. The desired slope information is given to the phase accumulator through its control bus which is digitally integrated by phase accumulator instantaneous phase information. Finally the digital phase word is converted to the digital amplitude word in LUT. As the information is changed at the control bus, the accumulator changes the address of the ROM thus selecting the other LUT wherein the data for different ramp amplitudes is stored.

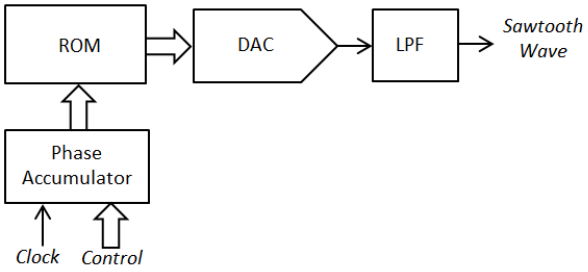


Fig 3: DDS based sawtooth generator

III. PROPOSED CIRCUIT

Fig. 4 shows the proposed circuit for digitally programmable sawtooth generator. It is a modification to the circuit shown in Fig. 1, where the counter is replaced by a programmable frequency divider as shown in Fig. 5. The programmable frequency divider accepts the reference clock (f_{in}) and generates the output clock at the output of multiplexer by selecting any of the four outputs of the counter (Q_1, Q_2, Q_3,Q_4) by the binary control word b_0 and b_1 connected at the selection lines of the multiplexer as shown in table 1. The waveforms obtained are shown in Fig. 6. As seen a division of $f_{in}/2^n$, i.e., 2, 4, 8, 16, can only be achieved.

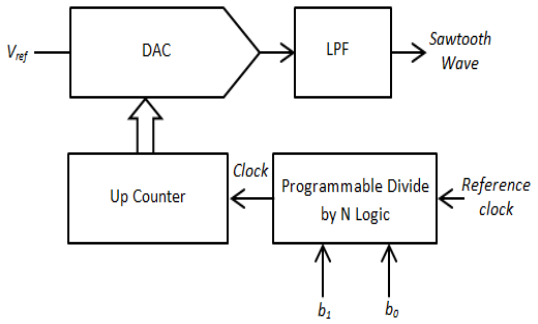


Fig 4: Proposed programmable sawtooth generator

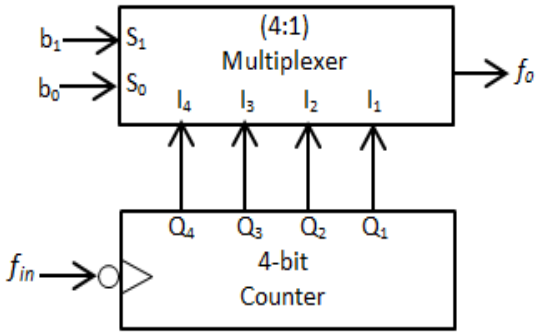


Fig 5: Programmable frequency divider

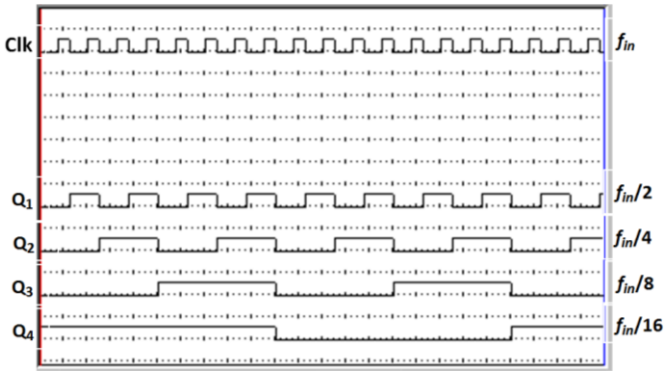


Fig 6: Data bits generated by counter

Table 1. Clock frequencies available at multiplexer

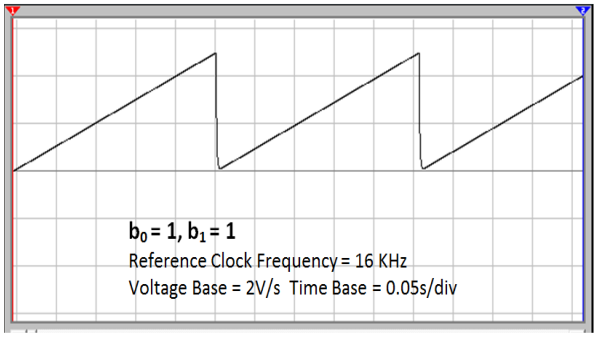
Control Word S_1	Control Word S_0	Counter Output	Output Frequency (f_o)
0	0	Q_1	$f_{in}/2$
0	1	Q_2	$f_{in}/4$
1	0	Q_3	$f_{in}/8$
1	1	Q_4	$f_{in}/16$

In order to obtain a division of f_{in}/n (where n=1, 2, 3, 4…..), a swallow counter based divider is required [5] which adds complexity and hence cost to the system. Any one of the ramp signals can be generated by applying a particular control word using the selection lines of the programmable frequency divider. The peak value of the ramp signal will be determined by the reference voltage applied to the DAC and the rate at which the ramp grows depends upon the frequency of the reference clock.

IV. EXPERIMENTAL RESULTS

The workability of the proposed circuit was tested in software simulations using Electronics Workbench. IC 7493 was used as a counter and 74153 as multiplexer. The results obtained are shown in Fig.7. The reference frequency (f_{in}) of 16 KHz was obtained from a function generator. In Fig. 7(d) where b_1=0 and b_0=0, an 8 KHz clock frequency at the output of the frequency divider is achieved and therefore the ramp grows rapidly as compared to other waves shown in Fig.

7(a–c), where the reference clock gets respectively divided by 16, 8 and 4. Thus by programming the circuit any slope of the ramp can be generated.



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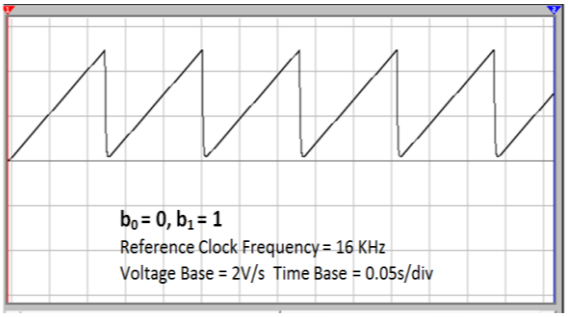

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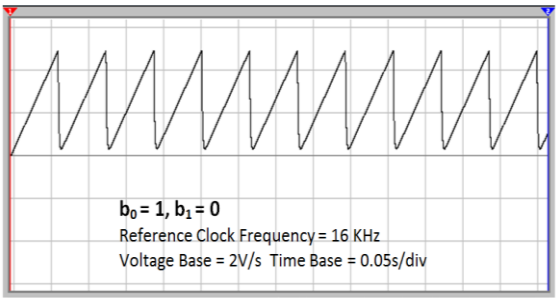
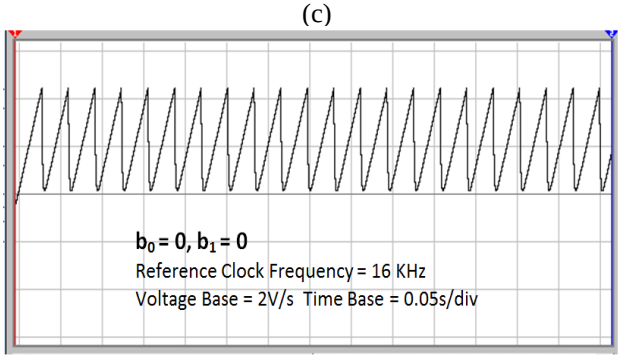


(c)



(d)

Fig 7: Waveforms generated by proposed circuit at (a) b_0 =1, b_1 =1; (b) b_0 = 0, b_1 = 1; (c) b_0 =1, b_1 = 0; (d) b_0 = 0, b_1=0

V. CONCLUSION

A simple circuit for programmable sawtooth generator is proposed in this paper. The circuit uses off-the- shelf components and can be used in the environments where ramp signals with different time periods are required. The circuit can be used in under graduate laboratories for demonstration of various experiments. The circuit can generate only few sets of ramp slops due to the limited programmability. The same can be overcome by using swallow counters.

REFERENCES

[1] Karnal, A, Tripati, K. C., and Prakash, "Inexpensive sawtooth wave; Adjustable and frequency-independent duty cycle square-wave oscillator," *IEEE Transactions on Instrumentation and Measurement*, vol. 36, no. 1, March 1987.

[2] Mallidi, "Ramp generator using operational amplifier based integrated and switched capacitor techniques," United States Patent, Patent No. US 8803569B1.

[3] Lee, M. C., and Chen, Y. C. 2017. Implementation of a ramp generator with Schmitt trigger circuit for PWM modulation applications Progress in Electromagnetics Research Symposium, Singapore.

[4] Ashwani, "Design of linear ramp generator for ADC," International conference on signal processing, communications and networking, Chennai-India, March, 2017.

[5] Lionel Cordesses, "Direct digital synthesis: A tool for periodic waveform generation," *IEEE signal processing magazine*, July, 2004.

[6] Faroze Ahmad, "On realization of a simple programmable frequency divider," *International Journal of Advanced Research in Electronics and Communication Engineer*ing, Vol. 6, No.8, 2017.