Five Level Diode Clamped Multi Level Inverter Based on Space Vector Modulation Technique

Arumalla Swathi[1], Vagicharla Karthik[2]
[1]*M.Tech Student, EEE Dept, Vasireddy Venkatadri Institute of Technology*
[2]*Assitant Professor, EEE Dept, Vasireddy Venkatadri Institute of Technology*

Abstract **--** With the development of high technology, inverter request higher capacity. However, the traditional two level inverter capacities of the power electronic devices have been difficult to achieve high power requirements. Therefore, the national science and technology workers continue to put forward a variety of excellent performance of new multilevel inverter topology. Space Vector Modulation (SVM) Technique has become the most popular and important PWM technique for three phase Voltage Source Inverters for the control of AC Induction, Brushless DC, Switched Reluctance and Permanent Magnet Synchronous Motors. This paper proposes implementation of Five Level Diode-Clamped Inverter based on Two Level Inverter using Space Vector Modulation technique. This paper presents a novel space vector pulse width modulation (SVPWM) scheme to reduce switching loss. Using this novel modulation strategy, the changing of switch states cause only one single phase voltage change every time. The simulation study of space vector modulation technique of two level Inverter reveals that space vector modulation technique utilizes DC bus voltage more efficiently and generates less harmonic distortion. The proposed scheme has been implemented by using MATLAB / SIMULINK and its feasibility has been verified by the experimental results.

Keywords *-- SVPWM, Diode – Clamped Inverter, Switching loss.*

I. INTRODUCTION

A device that converts DC into AC at desired output voltage and frequency is called an Inverter. Phase controlled converters when operated in the inverter mode are called line commutated inverters. But line commutated inverters require at the output terminals an existing AC supply which is used for their commutation. This means that line commutated inverters can't function as isolated AC voltage sources or as variable frequency generators with DC power at the input. Therefore, voltage level, frequency and waveform on the AC side of the line commutated inverters can't be changed. On the other hand, force commutated inverters provide an independent AC output voltage of adjustable voltage and adjustable frequency and have therefore much wider application. With increase of semiconductors technology, voltage source inverters have been extending its application in various area. Standard two level voltage source inverter consists of only one switching cell per phase. But in the field of high power driving systems, the level of direct current bus voltage constitutes an important limitation of the handled power. Another drawback is the very high dv/dt generated by the two level voltage source inverter. Multi-level inverters have more advantages than the standard two level inverters. Voltage harmonics are lower due to the increase of output voltage levels. Performance of multilevel inverters depends on the PWM algorithm. The triangular-sinusoidal and the hysteresis PWM are dissuaded in the case of multilevel inverters because they cannot deal with the major drawback of multilevel inverters is the DC-link capacitor voltage balancing. The space vector pulse with modulation provides superior harmonics capacity, and permits to solve the problem of unbalanced capacitors voltages by using the redundant states in the space voltage vector plane.

Multilevel inverters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a Limited maximum device rating. The best known topologies are the H-bridge cascaded inverter, the flying capacitor inverter, and the diode-clamped inverter. The most attractive features of multilevel inverters are as follows.

1. They can generate output voltages with extremely low distortion and dv/dt.
2. They draw input current with very low distortion.
3. They generate smaller common-mode (CM) voltage, thus reducing the stress of the motor bearing. In addition, we can use sophisticated modulation methods, then CM voltage can be eliminated.
4. They can operate with a lower switching frequency.

To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, which has equally divided zero voltage vectors describing a lower total harmonic distortion (THD)[1]. Although the complexity that presents the SVPWM strategy (many output vectors) compared with the carrier based PWM one, it remains the preferred seen that it reduces the power losses by minimizing the power electronic Devices switching frequency (limiting the minimum pulse width). For the high performance AC drive systems at increased power levels, high quality inverter

output is necessary for the low harmonic losses and torque pulsation. In the conventional two-level inverter configurations, the reduction of the harmonic contents of the inverter output current is achieved mainly by raising the switching frequency. However in the field of high voltage, high power application, the switching frequency of the power devices has to be restricted below l kHz, due to the increased switching losses, even in case of the HVJGBT and GCT. So the harmonic reduction by raised switching frequency of the two-level inverter becomes more difficult in high power applications. In addition, in two-level configurations, the DC link voltage of the two-level inverter is limited by the voltage ratings of the switching devices, so the problematic series connection of the switching devices is required to raise the DC link voltage. By series connection, the maximum allowable switching frequency has to be more lowered, thus the harmonic reduction becomes more difficult. From the aspect of the harmonic reduction and the higher voltage level. The harmonic contents of the Five-level inverter are less than that of Three-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the DC-link voltage. So the Five-level inverter topology is generally used in realizing the high performance, high voltage AC drive systems.

II. INVERTER TOPOLOGY

FIVE LEVEL INVERTER A device that converts DC voltage into AC voltage having five different level of output voltage is called as five level inverter.

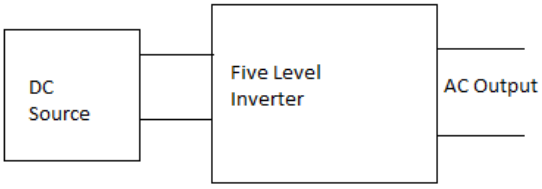


Fig.1. Block diagram of five level inverter

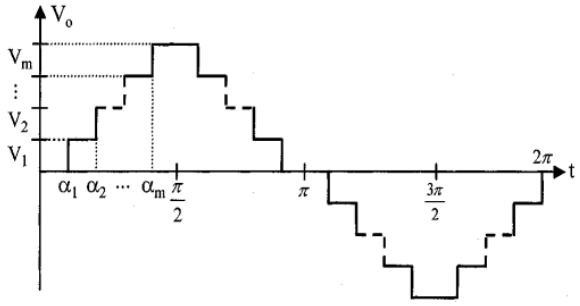


Fig.2. Waveform of five level inverter

Block Diagram and Waveform of Five level Inverter has shown in Fig 1 and Fig 2 respectively [2]. Fig. 3 shows diagram of a five-level diode clamping inverter. Each leg is composed of four upper and lower switches with anti-parallel diodes. Four series *dc*-link capacitors split the *dc*-bus voltage in half, and eighteen clamping diodes confine the voltages across the switches within the voltages of the capacitors. The necessary conditions for the switching states for the five-level inverter are that the *dc*-link capacitors should not be shorted, and the output current should be continuous. As indicated in Table I, each leg of the inverter can have five possible switching states, *P*1, *P2*, *O*, *N*1 or *N*2. When the top four switches *Sx*1, *Sx*2, *Sx*3 and *Sx*4 (*x* = *a*, *b*, *c*) are turned on, switching state is *P*2. When the switches *Sx*2, *Sx*3, *Sx*4 and *Sx*5 are turned on switching state is *P*1. When the switches *Sx*3, *Sx*4, *Sx*5 and *Sx*6 are turned on, the switching state is *O*. when the switches *Sx*4, *Sx*5, *Sx*6 and *Sx*7 are turned on, the switching state is *N*1. When the switches *Sx*5, *Sx*6, *Sx*7 and *Sx*8 are turned on, the switching state is N2. Fig.4 shows the space vector diagram for five-level inverter. The output pace vector is identified by combination of switching states *P*2, *P*1, *O*, *N*1 or *N*2 of the three legs. For example, in the case of *P*2*ON*1, the output terminals *a*, *b* and *c* have the potentials 2*E*, 0, and −*E* respectively. The output voltage vector can take only 61 discrete positions in the diagram because some switches states are redundant and create the same space vector. In Fig. 4, it is also indicated an arbitrary reference vector V∗ to be generated by the inverter.

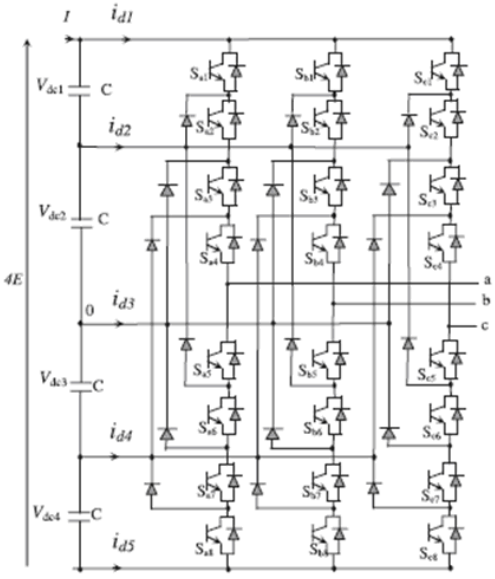


Fig.3 Configuration of five-level inverter

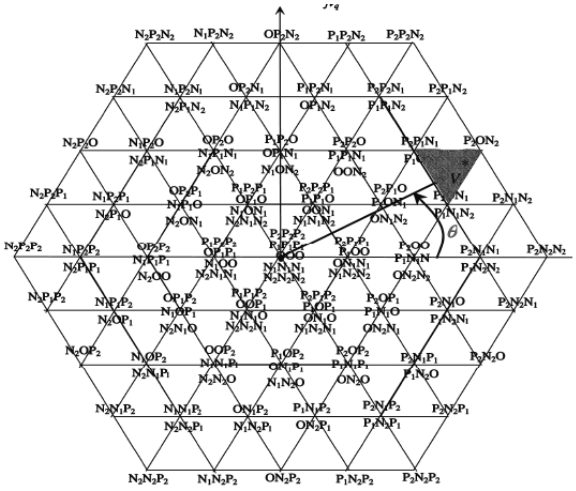


Fig. 4 Space vector diagram of five-level inverter

TABLE I: SWITCHING AND TERMINAL VOLTAGES OF FIVE-LEVEL INVERTER

States	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	V_{xo}
P2	1	1	1	1	0	0	0	0	2E
P1	0	1	1	1	1	0	0	0	E
O	0	0	1	1	1	1	0	0	0
N1	0	0	0	1	1	1	1	0	-E
N2	0	0	0	0	1	1	1	1	-2E

III. SPACE VECTOR MODULATION

A. *Basic Principle of Five level SVPWM Method*

The space vector diagram of multilevel inverter can be divided into different forms of sub-diagrams, in such a manner that the space vector modulation becomes more simple and easy to implement, as made in several works [3]–[7]. But these works do not reach a generalization of the two-level SVPWM to the case of multilevel inverters; either they divide the diagram into triangles, or into interfered geometrical forms. In this work, we present a simple and fast method that divides the space vector diagram of five-level inverter, within two steps, into several small hexagons, each hexagon being space vector diagram of two-level inverter, as shown in Fig. 5. This method is the extension of that presented in [8]-[10] for the case of three-level inverter. We have to make two simplifications: Firstly, the space vector diagram of five-level inverter is divided into six space vector diagrams of three-level inverters. Secondly, each one of these three-level inverter diagrams is divided into six space vector diagrams of two level inverters as shown in Fig. 6. Thus the space vector modulation of five-level inverter becomes very simple and similar to that of conventional two level inverter space vector modulation. To each this simplification, two steps have to be done. Firstly, from the location of a given reference voltage, one hexagon has to be selected among the hexagons. Secondly we translate the origin of the reference voltage vector towards the centre of the selected hexagon. These steps are explained in the next section.

B. *First Correction of Reference Voltage Vector*

Having the location of a given reference voltage vector, one hexagon is selected among the six small hexagons that contain the five-level space vector diagram Fig. 5. There exist some regions that are overlapped by two adjacent small hexagons. These regions will be divided in equality between the two hexagons. Each hexagon is identified by a number *S* defined as given in Table II.

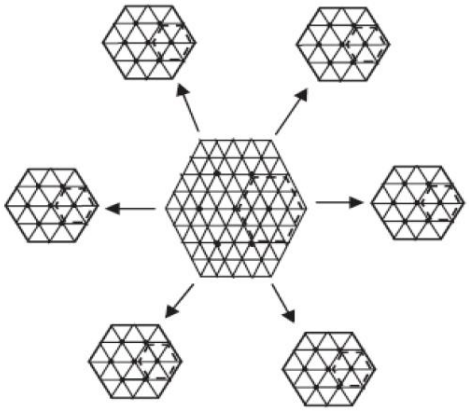


Fig.5: Decomposition of space vector diagram of five-level inverter to six hexagons

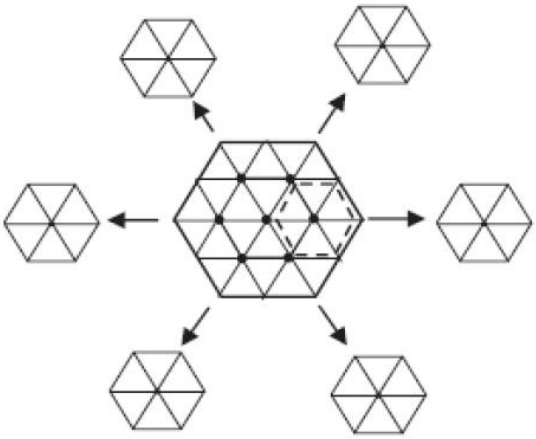


Fig. 6 Decomposition of space vector diagram of three-level inverter to six hexagons

TABLE II: SELECTION OF HEXAGONAL BASED ANGLE

Hexagon S	Location of reference voltage vector phase angle 'θ'
1	$-\frac{\pi}{6} < \theta < \frac{\pi}{6}$
2	$\frac{2\pi}{6} < \theta < \frac{\pi}{2}$
3	$\frac{3\pi}{2} < \theta < \frac{5\pi}{6}$
4	$\frac{4\pi}{6} < \theta < \frac{7\pi}{6}$
5	$\frac{7\pi}{6} < \theta < \frac{3\pi}{2}$
6	$\frac{3\pi}{2} < \theta < \frac{-\pi}{6}$

After selection of one hexagon, we make a translation of the reference vector ***V**** towards the center of this hexagon, as indicated in Fig. 7. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table III gives the components *d* and *q* of the reference voltage **V**3* after translation, for all the six hexagons. The index (3) or (5) above the components indicate three or five-level cases respectively

C. Second Correction of Reference Voltage Vector

Having the selected three-level inverter diagram and the location of the translated vector, one hexagon is selected among the six small hexagons that contain this three-level diagram Fig. 8 Here also the overlapped regions are equally divided between the two hexagons. After selection of one hexagon, we make a translation of the reference vector V***** towards the center of this hexagon, as indicated in Fig. 8. This translation is done by subtracting the center vector of the selected hexagon from the original reference vector. Table IV gives the components d and q of the reference voltage V2* after translation, for all the six hexagons. The index (2) or (3) above the components indicate two or three-level cases respectively.

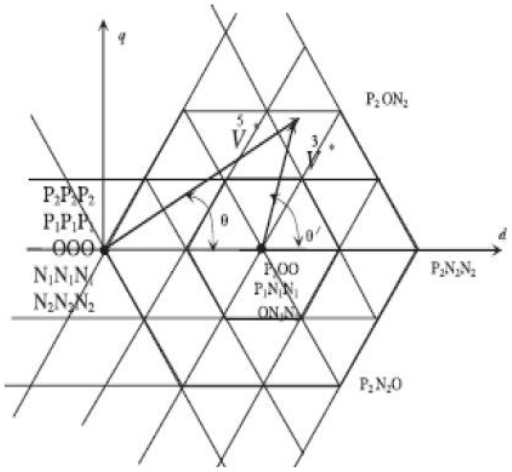


Fig.7: First Translation of Reference Voltage Vector

TABLE III: FIRST CORRECTION OF REFERENCE VOLTAGE VECTOR

S	V_d^{3*}	V_q^{3*}
1	V_d^{5*}-1/2cos(0)	V_q^{5*}-1/2sin(0)
2	V_d^{5*}-1/2cos($\pi/3$)	V_q^{5*}-1/2sin($\pi/3$)
3	V_d^{5*}-1/2cos($2\pi/3$)	V_q^{5*}-1/2sin($2\pi/3$)
4	V_d^{5*}-1/2cos(π)	V_q^{5*}-1/2sin(π)
5	V_d^{5*}-1/2cos($4\pi/3$)	V_q^{5*}-1/2sin($4\pi/3$)
6	V_d^{5*}-1/2cos($5\pi/3$)	V_q^{5*}-1/2sin($5\pi/3$)

TABLE IV: SECOND CORRECTION OF REFERENCE VOLTAGE VECTOR

s	V_d^{2*}	V_q^{2*}
1	V_d^{3*}-1/4cos(0)	V_q^{3*}-1/4sin(0)
2	V_d^{3*}-1/4cos($\pi/3$)	V_q^{3*}-1/4sin($\pi/3$)
3	V_d^{3*}-1/4cos($2\pi/3$)	V_q^{3*}-1/4sin($2\pi/3$)
4	V_d^{3*}-1/4cos(π)	V_q^{3*}-1/4sin(π)
5	V_d^{3*}-1/4cos($4\pi/3$)	V_q^{3*}-1/4sin($4\pi/3$)
6	V_d^{3*}-1/4cos($5\pi/3$)	V_q^{3*}-1/4sin($5\pi/3$)

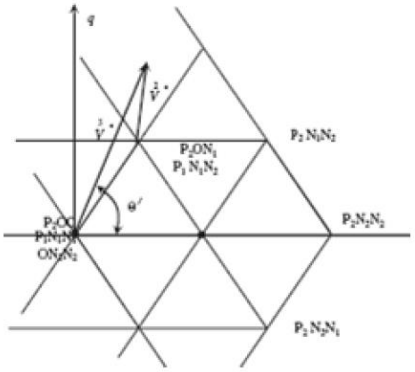


Fig.8: Second Translation of Reference Voltage Vector

D. Determination of Dwelling Times

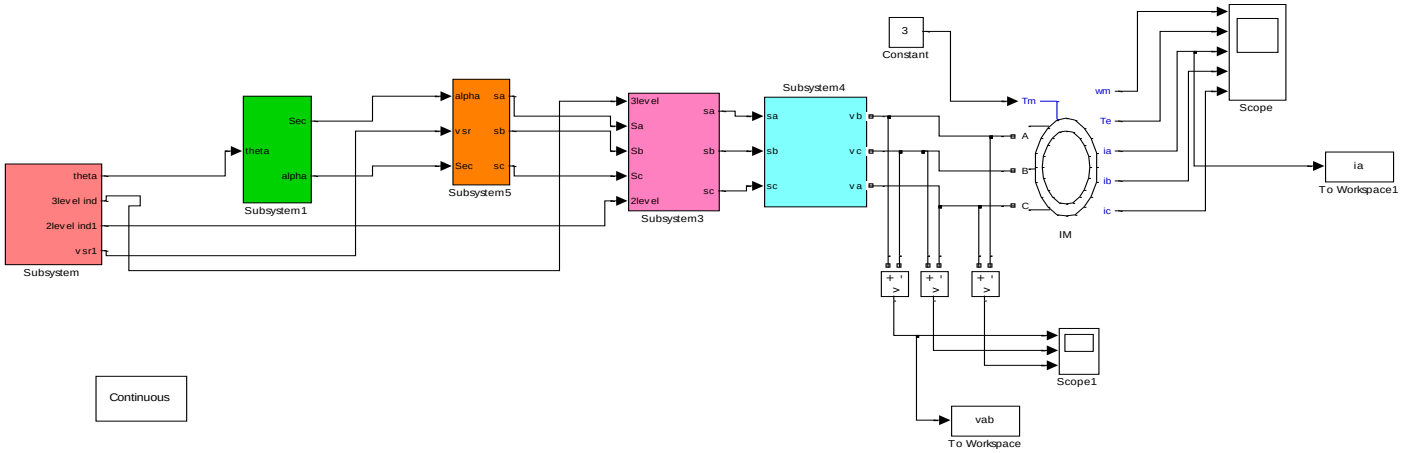
Once the corrected reference voltage V2* and the corresponding hexagon are determined, we can apply the conventional two-level space vector PWM method to calculate the dwelling times, the only difference between the two-level SVPWM and the five-level SVPWM is the factor 4 appearing at the first two equations as shown in (1). The remaining procedure is implemented like conventional two-level inverter SVPWM method and two level equivalent pulses are obtained.

$$T_1 = 4*\left[\frac{\left|\vec{V^{2*}}\right| \cdot T_s \cdot \sin\left(\frac{\pi}{3}-\alpha\right)}{\sin\left(\frac{\pi}{3}\right)}\right] \quad (1)$$

$$T_2 = 4*\left[\frac{\left|\vec{V^{2*}}\right| \cdot T_s \cdot \sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)}\right]$$

$$T_0 = T_s - T_1 - T_2$$

IV. SIMULATION MODEL



V. SIMULATION RESULTS

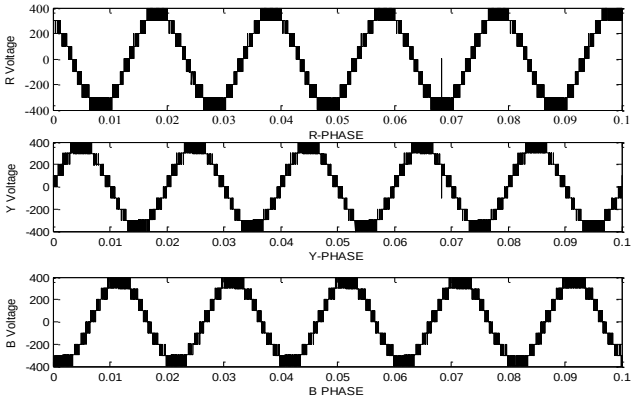


Fig 10. Five level voltages

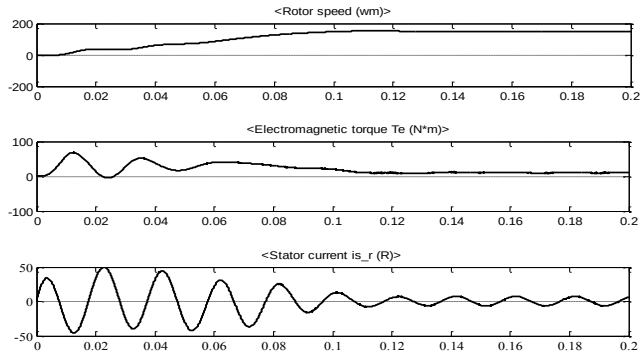


Fig.11: Five level ω, T, R-Phase current

In this work, Five Level diode clamped multilevel inverter of three phases simulated by using 5-level Space vector Pulse width modulation Technique (SVPWM) control inverter, and a simulation module by MATLAB/SIMULINK three phase multilevel inverters. The induction motor of 4 KW, 400V, 50Hz, 1430 RPM, Load Torque of 10 N-M has taken as three phase Load. The inverter is operated with a 5000Hz sampling Frequency with modulation index of 0.8. Fig 10 shows the five level line to line voltages with peak magnitude of 400V. Fig 11 shows the Steady state values of angular speed of 149 Rad/Sec, Torque of 10 N-m and R-Phase current of peak current of 10 A.

VI. CONCLUSION

In this paper, a simplification of the SVPWM applied for multilevel inverter is studied. To make this simplification, the SVPWM for five level inverter is reduced into SVPWM for three level inverter. In turn, the SVPWM for three level inverter is reduced to SVPWM for two level inverter. This simplification reduced considerably the computation time. The balancing of the capacitances voltages in the input side of the inverter can be made by rearranging the time distribution of the redundant voltage vectors. We can generalize this method to high order multilevel inverters.

VII. REFERENCE

[1] A. Nabea, i. Takahashi, and h. Akagi, "a new neutral-pointclamped pwm inverter," ieee transactions on industrial application, vol.ia- 17, no. 5, pp. 518-523, september/october 1981.

[2] Dj. Lalili, n. Lourci, e.m. berkouk, f. Boudjema j. Petzoldt and m.yasin dali "a simplified space vector pulse width modulation algorithm for five level diode clamping inverter" speedam 2006 international symposium on power electronics, electrical drives, automation and motion.

[3] Djaafer lalili, nabil lourci, el madjid berkouk, fares boudjema and j. Petzold- simplified space vector pulse width modulation algorithm for three level inverter with neutral point potential control"-research journal of applied sciences 1 (1-14):19-25,medwell online (2006)

[4] Jae hyeong seo, member, ieee, chang ho choi, member, ieee, and dong seok hyun, senior member, ieee- "a new simplified space–vector pwm method for three-level inverters" - ieee transactions on power electronics, vol. 16, no. 4, july 2001

[5] D. Lalili, e.m. berkouk, f. Boudjema, n. Lourci, t. Taleb, and j.petzold- simplified space vector pwm method for five-level inverter - eur. Phys. J. Appl. Phys. 40, 335–342 edp sciences (2007) the european physical journal applied physics -13 december 2007

[6] A.m. trzynadlowski, the field orientation principle in control of induction motors (kluwer academic publishers, 1994), isbn: 0-7923- 9420-8

[7] B.p. mcgrath, donald.g.holmes, thomas lipo, "optimised space vector switching sequences for multilevel inverters", ieee transactions on power electronics, vol.18,no.6, november 2003, pp 1293-1301.

[8] A.k.gupta and a.m.khabadkone " a general space vector pwm algorithm for multilevel inverters, including operation in over modulation range", ieee transactions on power electronics, vol.22, no.2, march 2007, pp517-526

[9] R.s.kanchan, m.r.baiju, k.k.mohapatra, p.p.ouseph and k.gopa kumar, " space vector pwm signal generation for multilevel inverters using only sampled amplitudes of reference phase voltages", proc.iee, vol.152, no.2, march 2005, pp297-309.

[10] P.f. seixas, m.a. severo mendes, p.donoso garia, a.m.n.lima, "a space vector pwm method for three-level voltage source inverters",proc. Apec, vol.1, 2000, pp 549-555.