8-Mbit (512K x 16) Static RAM

Part Number: DPA71051DV3302A

The DPA71051DV3302A is a high-performance CMOS Static RAM organized as 512K words by 16 bits.

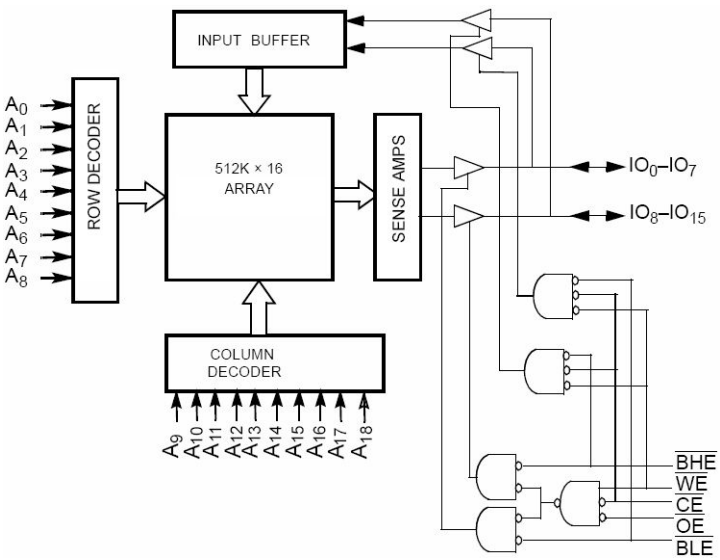
Writing to the device is accomplished by enabling the chip ($\overline{CE}_1$ LOW and CE_2 HIGH) while forcing the Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by enabling the chip by taking $\overline{CE}_1$ LOW and CE_2 HIGH while forcing the Output Enable ($\overline{OE}$) LOW and the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 through I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}.

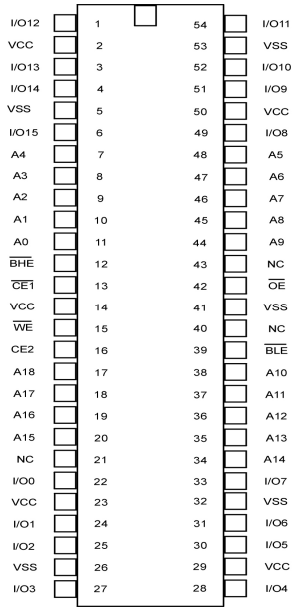
The Input/ Output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ HIGH/CE_2 LO), the outputs are

- **-55˚ to +125˚C operating temperature**
- **High speed**
  - **t_{AA} = 12 ns**
- **Low active power**
  - **I_{CC} = 110 mA @ 12 ns**
- **Low CMOS standby power**
  - **I_{SB2} = 20 mA**
- **Supply voltage**
  - **3.3 V dc**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$ and CE_2 features.**
- **54-pin SO ceramic flatpack, same footprint as 54-pin TSOP II**
- **Custom packaging is available**
- **This product uses Cypress CY7C1051DV33 die and is tested to meet military and space operational environment requirements.**

Logic Block Diagram



Pin Configuration



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