High Throughput BEC-1 Based 32*32 bit Vedic Multiplier

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Abstract **-** The speed of multiplier is an important concern in any DSP, MAC, ALU and all the signal processing operations. It is the impact of multiplier speed which determines the overall throughput of any DSP. Hence, implementation of fast, area and energy efficient designs is of utmost importance. This paper presents a high performance, high throughput BEC-1 based multiplier architecture. The paper also presents the fastest and efficient "urdhvatriyakbhyam technique" for multiplication which strikes a difference in regular array based multiplication itself. We have compared the area, speed and power of BEC-1 based Vedic multiplier with modified CLA based Vedic multiplier topologies. Proposed multiplier is coded in VHDL. Xillinx ISE 12.4 has been used for synthesis and ISIM has been used a simulation tool.

Keywords **-** *urdhvatriyakbhyam,Vedic multiplier, multioperand CSA, CLA, BEC-1, 32:16 MUX.*

I. INTRODUCTION

With latest advancements of VLSI the demand of portable DSP's have increased to a large extent. Multipliers are the fundamental component of DSP, microprocessor ALU. Multiplication process involves firstly the generation of partial products followed by their summation. Thus, increase in the number of bits to be multiplied is directly proportional to the number of adders being used [2]. Consequently, the speed of multiplier largely depends on the propagation delay of adders. Thus the need of fast multiplication gives rise to numerous algorithms. Array multiplication and booth encoding have been the most widely implemented techniques on digital hardware. In case of array multiplier, delay is the time taken by the signals to propagate through numerous gates present in multiplication array. For higher order multiplication delay increases tremendously. Similarly booth encoding multiplier takes 2n clock cycles to calculate LSB of product which makes it slower [3]. Hence, there is a need of more sophisticated and promising multipliers. Vedic multipliers have proved the most challenging solution to this problem.
Proposed BEC-1 based vedic multiplier exploits "urdhvatriyakbhyam" sutra. It is simply vertically and crosswise algorithm which involves parallel generation of partial products and involves least number of steps for calculation thus reducing logic and routing delay of the design and thus improving the overall performance of the digital system. Urdhvatriyakbhyam technique effectively handles larger operands. Thus, overcoming the shortcomings of an array multiplier.

II. VEDIC SUTRAS

The word 'Vedic' is derived from the word 'veda' which means the store-house of all knowledge. Vedic mathematics deals with 16 sutras [1]. The paper gives a brief introduction of "urdhvatriyakbhyam sutra' since it forms the basis of proposed multiplier

1. Anurupye Shunyamanyat– If one is in ratio, the other is zero
2. Chalana-Kalanabyham– Differences and Similarities
3. Ekadhikina Purvena– By one more than the previous one
4. Ekanyunena Purvena– By one less than the previous one
5. Gunakasamuchyah– The factors of the sum is equal to the sum of the factors
6. Gunitasamuchyah– The product of the sum is equal to the sum of the product
7. Nikhilam Navatashcaramam Dashatah– All from 9 and the last from 10
8. Paraavartya Yojayet– Transpose and adjust
9. Puranapuranabyham– By the completion or noncompletion.
10. Sankalana-vyavakalanabhyam– By addition and by subtraction
11. Shesanyankena Charamena– The remainders by the last digit
12. Shunyam Saamyasamuccaye– When the sum is the same that sum is zero
13. Sopaantyadvayamantyam– The ultimate and twice the penultimate
14. Urdhva Tiryakbyham– Vertically and crosswise.
15. Vyashtisamanstih– Part and Whole
16. Yaavadunam– Whatever the extent to fits deficiency

A. Urdhvatriyakbhyam Sutra

This sutra is based on "Vertically and Crosswise" technique. There is striking difference in method of computation of Vedic multiplier as it handles an array of large numbers (NXN) bits by dividing them into small [N/2 X N/2] for parallel generation of partial products. Thus, it performs multiplication with minimum number of steps which in-turn reduces the delay and hardware requirements. The Vedic multiplier is independent of clock frequency as partial product and their summation occur simultaneously. We know that, Dynamic power $P= CV^2f$ is directly proportional to switching frequency of clock. Hence, the dynamic power consumption of the vedic multiplier also reduces thus, making vedic multiplication an energy efficient approach. Figure 1 shows the line diagram for the multiplication of two 4-bit numbers.

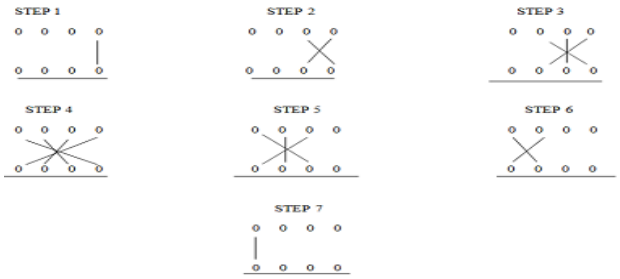

Fig. 1. Existing 32*32 BIT Vedic Multiplier Architectures

III. EXISTING 32* 32 BIT VEDIC MULTIPLIER TOPOLOGIES

A. *Conventional 32*32 bit vedic multiplier*

Conventional 32*32 bit vedic multiplier [4,5] shown in fig2 is comprised of three 32-bit Ripple carry adders to generate final product. It involves a cascaded chain of N-1 full for parallel addition. Though ripple carry adders consume less power and have compact layout but they are not efficient for large bit numbers. Since, the delay of RCA increases linearly with increase in the lengths of addend and augends. One of the major factor affecting its speed is that it has to wait for the carry to ripple from previous state to next state for its further operation. Hence, its speed gets restricted. Combinational delay of this approach was found to 42.268 ns.

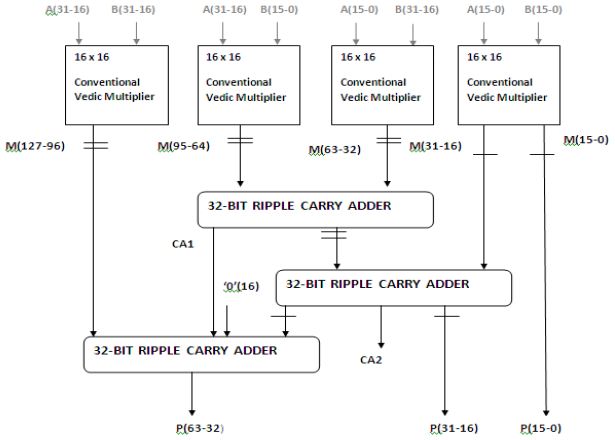

Fig. 2. 32*32 Bit Conventional Vedic Multiplier

B. *Carry look ahead adder based Vedic multiplier*

Vedic multiplier based on CLA [7] as shown in Fig 3 has an upper hand over RCA as they are designed to overcome the latency introduced due to carry rippling effect of carry bits in RCA. This adder is independent of the carry generated in the preceding stage and depends only on the data bits of addend and augends to decide whether or not carry will be generated. Thus, CLA adder eliminates the carry delay by reducing the number of gates through which the carry needs to propagate hence, area reduces[8]. The adder has 3 stages. Carry generation' Propagation block followed by carry and sum generation units.

Gi = Ai and Bi……carry generate block

Pi = Ai xor Bi……carry propagate block

$C_i = G_i + P_i C_{i-1}$.....carry generation

$S_i = A_i \text{ xor } B_i C_{i-1}$……...Sum generation

The modified Vedic multiplier has 3 carry look ahead adder of variable length. Combinational delay is found to be 46.762 ns which is almost same as RCA based adder but this design occupies less number of slices and CLB as compared to conventional architecture.

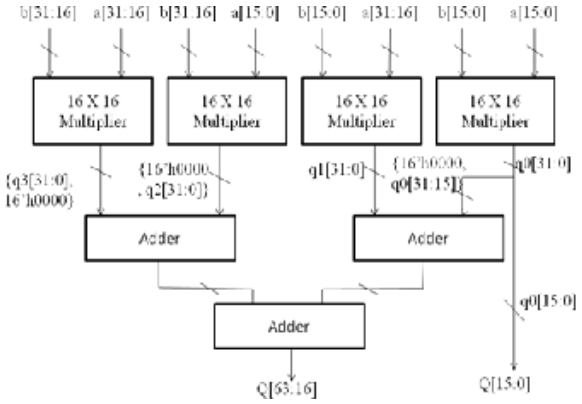

Fig. 3. CLA-based 32*32 bit vedic multiplier

C. *Modified Carry look ahead adder based Vedic multiplier*

The modified architecture of 16 bit multiplier was proposed [6] which has been extended in the paper for 32 bit multiplicationas shown in fig 4. Modified architecture uses only two 32-Bit CLA unlike the above architecture which uses three CLA. 16* 16 bit vedic multipliers are used to generate 32 bit partial products. These partial products are then added by CLA arrangement to generate final product bits. Finally a half adder assembly is employed to generate the MSB of final product. The above architecture was Modeled and coded in VHDL using Xillinx 12.1. Combinational delay was observed to be 38.885 ns. Hence, proposed architecture is fastest and lowest power consuming vedic multiplier when compared to all existing architecture. It occupies only 2031 slices which makes it even more area efficient.

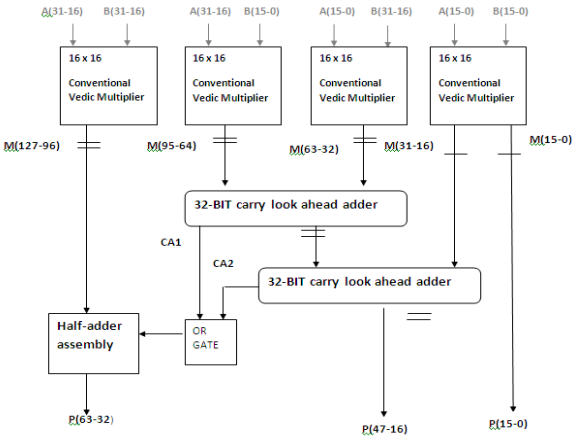

Fig. 4. Modified vedic multiplier

IV. PROPOSED BEC-1 BASED HIGH PERFORMANCE VEDIC MULTIPLIER

Hardware implementation of Proposed architecture in[10] has been extended to 32*32 bit vedic multiplier. It includes following in divided into following subparts as shown in fig 5.

a. 16*16 bit Vedic multiplier

b. Multi-operand carry save adder

c. Binary to Excess-1 code converter

d. 32:16 MUX.

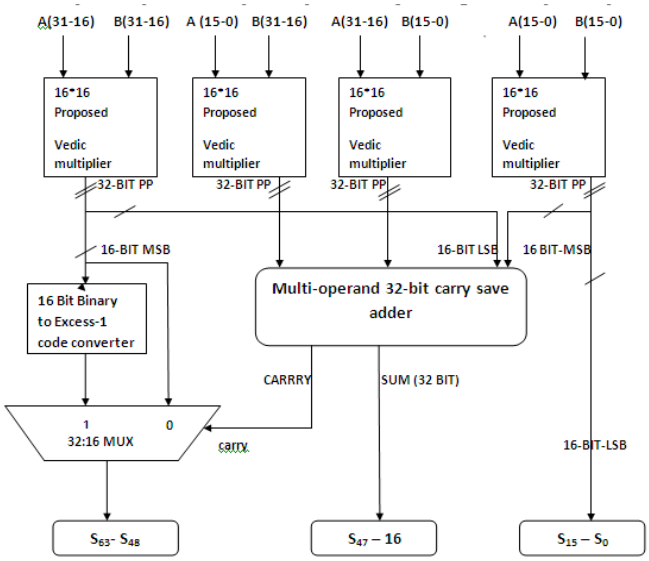

Fig. 5. Proposed 32*32 BEC-1 based vedic multiplier

The first step in the designing of 32*32 block will be grouping the 16-bits of each 32 bit input. The lower and the upper group of 16-bits will form vertical and crosswise product terms[6]. Each 16-bit pair will be handled by separate 16*16 bit Vedic multiplier to form 32-bit partial products by applying urdhvatriyakbhyam technique..

These 32-bit partial products are then provided as an input to the multi-operand carry save adder to generate final product.

The 32-bit multi-operand CSA consists of 32 disjoint full adders [3] which unlike, RCA does not have carry chaining. Each full adder results in a single bit sum and a single bit carry. Hence it generates n-bit partial sum and partial carry. Therefore, converts a problem of addition of 3 input numbers to 2 numbers [8]. Two CLA in modified 32-bit CLA based vedic multiplier are compressed to single Multi-operand carry save adder in the proposed BEC-1 based multiplier. Two 32-bit CLA together gives delay of 20.634 ns whereas 32-bit multi-operand CSA is faster and gives a delay of 15.553 ns. Hence, the proposed vedic multiplier is fastest. CLA also have a disadvantage of occupying large area as no. of bits increase.

Finally the carry generated by the CSA is given as an input to the selection line of 32:16 MUX. If Cin=1, then final output is taken from Binary to excess one code converter and if Cin=0 then, final output is same as the MSB of partial product generated by 16*16 bit vedic multiplier. BEC-1[9] shown in fig 6 is used as a key element in this proposed multiplier as it reduces the delay and occupies less area compared to full adder. Thus, the overall performance of 32*32 bit proposed vedic multiplier is enhanced. It provides a delay of 34.678 ns which is better than any of the existing topologies.

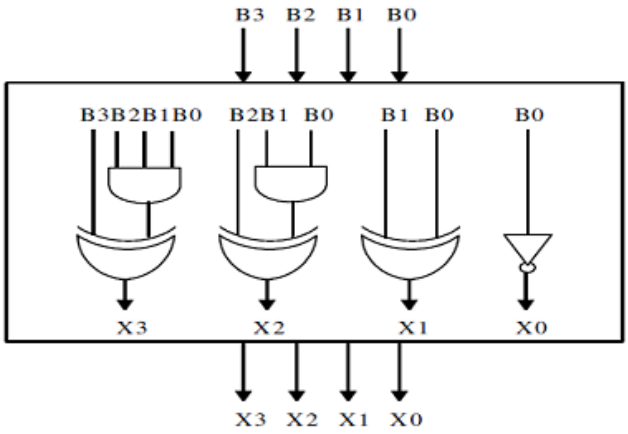

Fig. 6. binary to excess-1 converter

V. SIMULATION AND RESULTS

Simulation and synthesis is done using Xlinx ISE 12.4, and ISIM selecting device Spartan-3 FPGA (XC3S400-PQ208).Power analysis has been done using xillinx power analyzer.

Here, the figure 8 shows RTL- schematic and figure 7 shows the test bench wave form generated by Xillinx ISE 12.4 and ISIM. Table.1 shows the comparison of BEC-1 based vedic multiplier with Conventional vedic multiplier and CLA-based Vedic multiplier and modified CLA- based vedic multiplier.

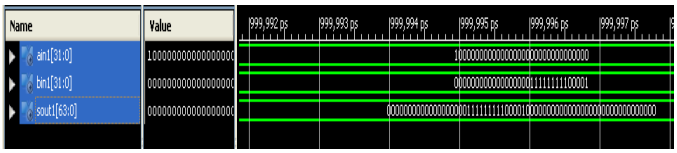

Fig. 7. ISIM waveform of BEC-1 based 8*8 vedic multiplier

TABLE I: COMPARISION OF BEC-1 BASED MULTIPLIER WITH EXISTING TOPOLOGY

Vedic architecture	Delay	logic delay	Route delay	Slice utiliza -tion	4i/p LUT utiliza -tion	Power (mW)
Conventional architecture	42.268 ns	18.217 ns	24.051 ns	2217	4319	160
CLA -based existing architecture	46.762 ns	20.954 ns	25.880 ns	2148	4168	154
Modified CLA- based architecture	38.885 ns	17.242 ns	21.613 ns	2031	3940	146
Proposed BEC-1 based Architecture	**34.678 ns**	**15.579 ns**	**19.099 ns**	**1881**	**3664**	**140**

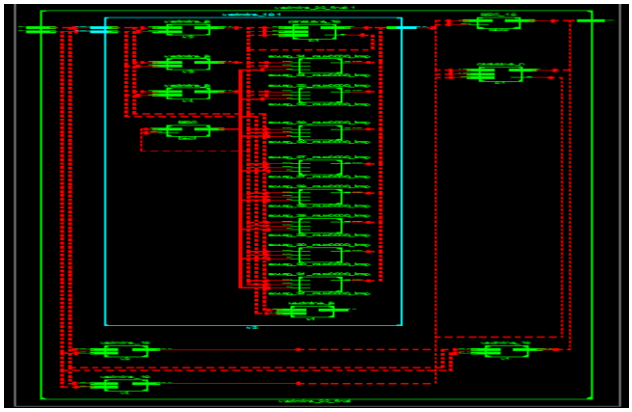

Fig. 8. RTL schemetic of BEC-1 based vedic multiplier

VI. CONCLUSION

Multiplication is the key operation in all arithmetic, logic and signal processing operations hence, we need to implement an area wise, energy- wise speedy multiplier. The proposed BEC-1 based vedic multiplier gives reduced logic and route delay of 15.579 ns and 19.099 ns respectively. It occupies 1881 out of 3584 slices available in Spartan 3 which is less than the area requirements of any of the existing multiplier architecture. The Dynamic power consumption is 140 mW as calculated by the XPA tool. Thus, the results predict the the proposed multiplier fulfills are major aims of reduced delay, reduces area and reduced power consumption.

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