REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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NOT TO BE USED FOR PROCUREMENT

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22												

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

APPROVED BY

DRAWING APPROVAL DATE

REVISION LEVEL

MICROCIRCUIT, MEMORY, DIGITAL, 1M X 18 SYNCHRONOUS STATIC RANDOM ACCESS MEMORY (SRAM), 1.8 V, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-08237**

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	08237	01	N	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes N, Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Maximum operating speed
01		1M X 18 CMOS SRAM	250 MHz
02		1M X 18 CMOS SRAM	200 MHz
03		1M X 18 CMOS SRAM	167 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N	Certification and qualification to MIL-PRF-38535 for plastic encapsulated microcircuit (PEM)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	165	Fine pitch ball grid array (FBGA)

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q and V.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.6.2 herein).

1.3 Absolute maximum ratings. 2/

Supply voltage range (V_{DD})	-0.5 V dc to + 2.9 V dc
Voltage range on any input	-0.5 V dc to V_{DD} + 0.3 V dc
Voltage range on any output pin	-0.5 V dc to V_{DDQ} + 0.3 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	
01	3.26 W
02	2.70 W
03	2.29 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	5.91 °C/W 3/
Junction temperature (T_J)	+140°C 4/
Output current	20 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	1.7 V dc to 1.9 V dc
Supply voltage to outputs (V_{DDQ})	1.4 V dc to V_{DD}
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH})	V_{REF} + 0.1 V dc to V_{DDQ} + 0.3 V dc 5/ 6/
Input low voltage range (V_{IL})	-0.3 V dc to V_{REF} – 0.1 V dc 5/ 6/
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Tested initially and after any design or process changes that may affect these parameters.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
5/ Overshoot: $V_{IH}(AC) < V_{DDQ}$ +0.85V (Pulse width less than $t_{CYC}/2$), Undershoot: $V_{IL}(AC) > -1.5V$ (Pulse width less than $t_{CYC}/2$).
6/ $V_{REF}(Min) = 0.68V$ or $0.46V_{DDQ}$, whichever is larger. $V_{REF}(Max) = 0.95V$ or $0.54V_{DDQ}$, whichever is smaller.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 -	IC Latch-Up Test.
JEDEC Solid State Product Outline MO-216 -	Thin Profile, Square and Rectangular, Ball Grid Array Family, 1.00 & 0.80MM Pitches.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests are used to test this device. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes N, Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q and V shall be in accordance with MIL-PRF-38535

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes N, Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q and V, the requirements of MIL-PRF-38535.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Output HIGH Voltage 4/	V_{OH}		1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Output LOW Voltage 5/	V_{OL}		1, 2, 3	All	$V_{DDQ}/2$ - 0.12	$V_{DDQ}/2$ + 0.12	V
Output HIGH Voltage	$V_{OH(LOW)}$	I_{OH} = -0.1 mA, nominal impedance	1, 2, 3	All	V_{DDQ} -0.2	V_{DDQ}	V
Output LOW Voltage	$V_{OL(LOW)}$	I_{OL} = 0.1 mA, nominal impedance	1, 2, 3	All	V_{SS}	0.2	V
Input HIGH Voltage	V_{IH}		1, 2, 3	All	V_{REF} +0.1	V_{DDQ} +0.3	V
Input LOW Voltage	V_{IL}		1, 2, 3	All	-0.3	V_{REF} -0.1	V
Input Leakage Current	I_X	$GND \le V_I \le V_{DDQ}$	1, 2, 3	All	-5	5	uA
Output Leakage Current	I_{OZ}	$GND \le V_I \le V_{DDQ}$, output disabled	1, 2, 3	All	-5	5	uA
Input Reference Voltage 6/	V_{REF}	Typical value = 0.75 V	1, 2, 3	All	0.68	0.95	V
V_{DD} Operating Supply Current	I_{DD}	V_{DD} = max, I_{OUT}=0 Ma $f = f_{MAX} = 1/t_{CYC}$	1, 2, 3	01		1125	mA
				02		930	mA
				03		790	mA
Automatic CE Power-Down Current - TTL Inputs	I_{SB1}	V_{DD} = max, both ports deselected, inputs static $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$ $f = f_{MAX} = 1/t_{CYC}$	1, 2, 3	01		350	mA
				02		310	mA
				03		290	mA
Input Capacitance 1/	C_{IN}	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8 V_{DDQ} = 1.5V	4	All		5	pF
Clock Input Capacitance 1/	C_{CLK}		4	All		6	pF
Output Capacitance 1/	C_{OUT}		4	All		7	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
K Clock and C Clock Cycle Time	t_{CYC}	See Figure 5 as applicable. 7/ 8/	9, 10, 11	01	4.0	6.3	ns
				02	5.0	7.9	
				03	6.0	7.9	
Input Clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH 1/	t_{KH}		9, 10, 11	01	1.6	---	ns
				02	2.0	---	
				03	2.4	---	
Input Clock (K/$\overline{K}$ and C/$\overline{C}$) LOW 1/	t_{KL}		9, 10, 11	01	1.6	---	ns
				02	2.0	---	
				03	2.4	---	
K Clock Rise to $\overline{K}$ Clock Rise and C to $\overline{C}$ Rise (rising edge to rising edge)	$t_{KH\overline{K}H}$		9, 10, 11	01	1.8	---	ns
				02	2.2	---	
				03	2.7	---	
K/$\overline{K}$ Clock Rise to C/$\overline{C}$ Clock Rise (rising edge to rising edge	t_{KHCH}		9, 10, 11	01	0.0	1.8	ns
				02	0.0	2.2	
				03	0.0	2.7	
Address Setup to K Clock Rise	t_{SA}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	
Control Setup to K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	t_{SC}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	
Double Data Rate Control Setup to Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$,$\overline{BWS_3}$)	t_{SCDDR}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	
$D_{[X:O]}$ Setup to Clock (K/$\overline{K}$) Rise	t_{SD}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	
Address Hold after K Clock Rise	t_{HA}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	
Control Hold after K Clock Rise ($\overline{RPS}$, $\overline{WPS}$)	t_{HC}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	
Double Data Rate Control Hold after Clock (K/$\overline{K}$) Rise ($\overline{BWS_0}$, $\overline{BWS_1}$, $\overline{BWS_2}$,$\overline{BWS_3}$)	t_{HCDDR}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
$D_{[X:0]}$ Hold after Clock (K/$\overline{K}$) Rise	t_{HD}		9, 10, 11	01	0.35	---	ns
				02	0.4	---	
				03	0.5	---	
C/$\overline{C}$ Clock Rise (or K/$\overline{K}$ in Single Clock Mode) to Data Valid	t_{CO}		9, 10, 11	01	---	0.45	ns
				02	---	0.45	
				03	---	0.50	
Data Output Hold after Output C/$\overline{C}$ Clock Rise (Active to Active)	t_{DOH}		9, 10, 11	01	-0.45	---	ns
				02	-0.45	---	
				03	-0.50	---	
C/$\overline{C}$ Clock Rise to Echo Clock Valid	t_{CCQO}		9, 10, 11	01	---	0.45	ns
				02	---	0.45	
				03	---	0.50	
Echo Clock Hold after C/$\overline{C}$ Clock Rise 1/	t_{CQOH}		9, 10, 11	01	-0.45	---	ns
				02	-0.45	---	
				03	-0.50	---	
Echo Clock High to Data Valid 1/	t_{CQD}		9, 10, 11	01	---	0.30	ns
				02	---	0.35	
				03	---	0.40	
Echo Clock High to Data Invalid 1/	t_{CQDOH}		9, 10, 11	01	-0.30	---	ns
				02	-0.35	---	
				03	-0.40	---	
Output Clock (CQ/$\overline{CQ}$) High 1/ 11/	t_{CQH}		9, 10, 11	01	1.55	---	ns
				02	1.95	---	
				03	2.45	---	
CQ Clock Rise to $\overline{CQ}$ Clock Rise (rising edge to rising edge) 1/ 11/	$t_{CQH\overline{CQ}H}$		9, 10, 11	01	1.55	---	ns
				02	1.95	---	
				03	2.45	---	
Clock (C/$\overline{C}$) Rise to High Z (Active to High Z) 1/ 9/10/	t_{CHZ}		9, 10, 11	01	---	0.45	ns
				02	---	0.45	
				03	---	0.50	
Clock (C/$\overline{C}$) Rise to Low Z 1/ 9/10/	t_{CLZ}		9, 10, 11	01	-0.45	---	ns
				02	-0.45	---	
				03	-0.50	---	
Clock Phase Jitter 1/	$t_{KC\ Var}$		9, 10, 11	01	---	0.20	ns
				02	---	0.20	
				03	---	0.20	

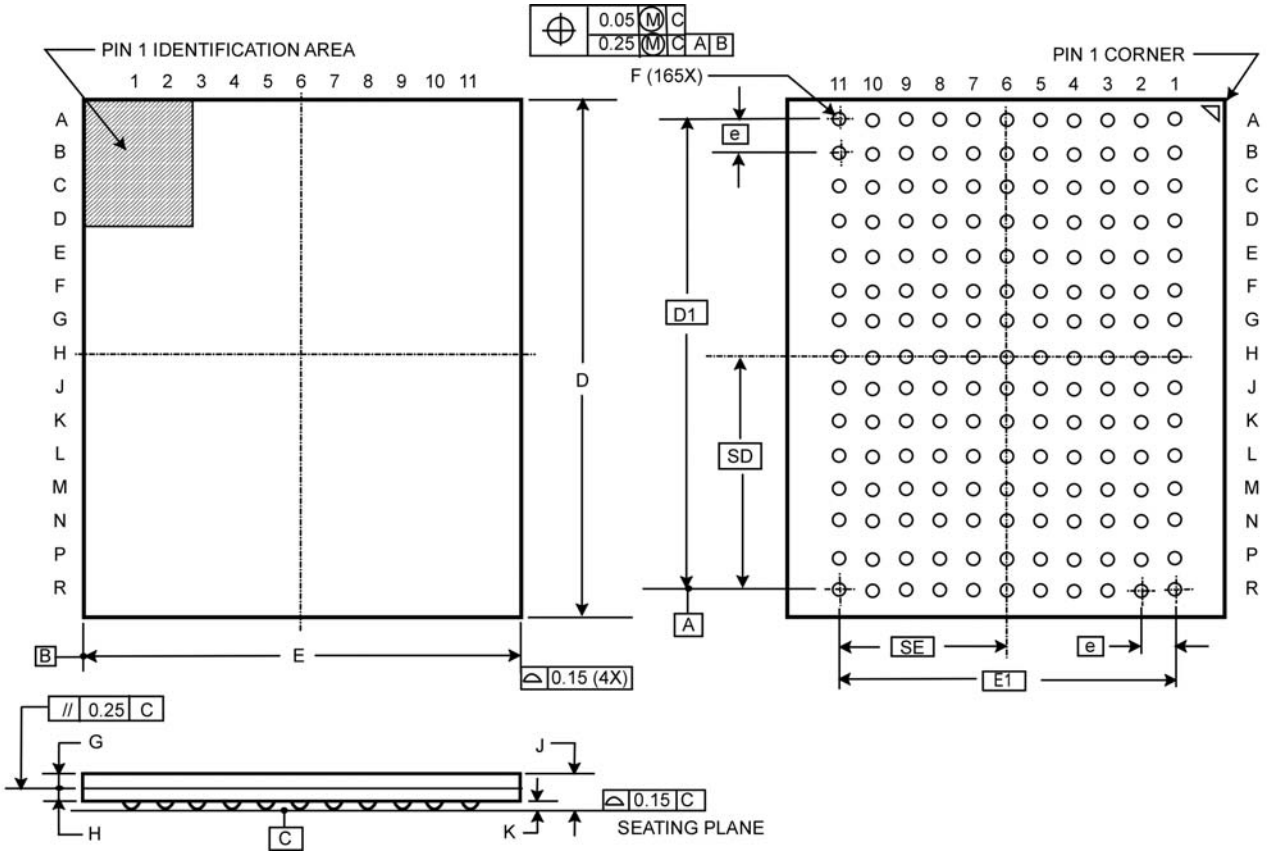
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55° \le T_C \le 125°C$ $1.7\ V \le V_{DD} \le 1.9\ V$ $1.4V \le V_{DDQ} \le V_{DD}$ Unless Otherwise Specified 2/ 3/	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
DLL Lock Time (K,C)	$t_{KC\ Lock}$		9, 10, 11	01	1024	---	cycles
				02	1024	---	
				03	1024	---	
K Static to DLL Reset	$t_{KC\ Reset}$		9, 10, 11	01	30	---	ns
				02	30	---	
				03	30	---	

1/ Tested initially and after any design or process changes that may affect these parameters.
2/ All voltage referenced to ground.
3/ Power up: Assumes a linear ramp from 0V to V_{DD}(min) within 200 ms. During this time, $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
4/ Outputs are impedance controlled. $I_{OH} = -(V_{DDQ}/2)/(RQ/5)$ for values of $175\Omega \le RQ \le 350\Omega$.
5/ Outputs are impedance controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $175\Omega \le RQ \le 350\Omega$.
6/ V_{REF}(min) = 0.68V or $0.46V_{DDQ}$, whichever is larger, V_{REF}(max) = 0.95V or $0.54V_{DDQ}$, whichever is smaller
7/ Unless otherwise noted, test conditions assume signal transition time of 2V/ns, timing reference levels of 0.75V, V_{REF} = 0.75V, RQ = 250Ω, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure 4(a), AC test loads.
8/ When a part with a maximum frequency above 167MHz is operating at a lower clock frequency, it requires the input timing of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
9/ t_{CHZ} and t_{CLZ} are specified with a load capacitance of 5 pF as in Figure 4(b), AC test loads. Transition is measured ±100 mV from steady-state voltage.
10/ At any voltage and temperature t_{CHZ} is less than t_{CLZ} and t_{CHZ} is less than t_{CO}.
11/ These parameters are extrapolated from the input timing parameters ($t_{KH\bar{K}H}$ -250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps ($t_{KC\ Var}$) is already included in the $t_{KH\bar{K}H}$). These parameters are only guaranteed by design and are not tested in production.

Case X (see notes)



Symbol	Millimeters			Symbol	Millimeters		
	Min	Nom	Max		Min	Nom	Max
D	14.90	15.00	15.10	H	0.31	0.36	0.41
D1	-	14.00 BSC	-	J	-	-	1.40
E	12.90	13.00	13.10	K	0.29	0.35	0.41
E1	-	10.00 BSC	-	SD	-	7.00 BSC	-
e	-	1.00 BSC	-	SE	-	5.00 BSC	-
F	0.44	0.50	0.64	N	165		
G	0.48	0.53	0.58				

NOTES:
1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.
2. Ref: JEDEC MO-216 for ball pattern.

FIGURE 1. Case outlines.

Pin Configuration

Device Type= All											
Case Outline= X											
	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC	NC	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC	$\overline{RPS}$	A	NC	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	A	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{CCQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Pin Definitions

Pin	Name	Function
$D_{[17:0]}$	Input-Synchronous	**Data Input Signals**. Samples on the rising edge of K and $\overline{K}$ clocks during valid write operations.
$\overline{WPS}$	Input-Synchronous	**Write Port Select- Active LOW**. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting deselects the write port. Deselecting the write port ignores $D_{[17:0]}$.
$\overline{BWS_0}$ $\overline{BWS_1}$	Input-Synchronous	**Byte Write Select 0 and 1- Active LOW**. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. $\overline{BWS_0}$ controls $D_{[8:0]}$, $\overline{BWS_1}$ controls $D_{[17:9]}$. All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and it is not written into the device.
A	Input-Synchronous	**Address Inputs.** Sampled on the rising edge of the K (Read address) and $\overline{K}$ (Write address) clocks during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 1M x 18 (2 arrays each of 512K x 18). Therefore, only 19 address inputs are needed to access the entire memory array. These inputs are ignored when the appropriate port is deselected.
$Q_{[17:0]}$	Output-Synchronous	**Data Output Signals.** These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during read operations, or K and $\overline{K}$ when in single clock mode. When the read port is deselected, $Q_{[17:0]}$ are automatically tri-stated.

FiIGURE 2. Terminal Connections

Pin Definitions. – continued.

Pin	Name	Function
$\overline{RPS}$	Input-Synchronous	**Read Port Select- Active LOW.** Sampled on the rising edge of positive input clock (K). When active, a read operation is initiated. Deasserting deselects the read port. When deselected, the pending access is allowed to complete and the output drivers are automatically tri-stated following the next rising edge of the C clock. Each read access consists of a burst of two sequential transfers.
C	Input Clock	**Positive Input Clock for Output Data.** C is used in conjunction with $\overline{C}$ to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller.
$\overline{C}$	Input Clock	**Negative Input Clock for Output Data.** $\overline{C}$ is used in conjunction with C to clock out the read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller.
K	Input Clock	**Positive Input Clock Input**. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[17:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	**Negative Input Clock Input.** $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[17:0]}$ when in single clock mode.
CQ	Echo Clock	**CQ Referenced with Respect to C.** This is a free-running clock and is synchronized to the input clock for output data (C) of the QDR-II. In the single clock mode, CQ is generated with respect to K. The timings for the echo clocks is shown in the Switching Characteristics (Table I).
$\overline{CQ}$	Echo Clock	**$\overline{CQ}$ Referenced with Respect to $\overline{C}$.** This is a free-running clock and is synchronized to the input clock for output data ($\overline{C}$) of the QDR-II. In the single clock mode, $\overline{CQ}$ is generated with respect to $\overline{K}$. The timings for the echo clocks is shown in the Switching Characteristics (Table I).
ZQ	Input	**Output Impedance Matching Input.** This input is used to tune the device outputs to the system data bus impedance. CQ, $\overline{CQ}$, and $Q_{[17:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
$\overline{DOFF}$	Input	**DLL Turn Off- Active LOW.** Connecting this pin to ground turns off the DLL inside the device. For normal operation, this pin can be connected to a pull up through a 10 KΩ or less pull up resistor. The device behaves in DDR-I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with QDR-I timing.
TDO	Output	**TDO for JTAG.**
TCK	Input	**TCK Pin for JTAG.**
TDI	Input	**TDI Pin for JTAG.**
TMS	Input	**TMS Pin for JTAG**
NC	N/A	**Not Connected to the Die.** Can be tied to any voltage level.
V_{REF}	Input-Reference	**Reference Voltage Input.** Static input used to set reference level for HSTL inputs, Outputs, and AC measurement points.
V_{CC}	Power Supply	**Power Supply Inputs to the Core of the Device.**
V_{SS}	Ground	**Ground for the Device.**
V_{DDQ}	Power Supply	**Power Supply Inputs for the Outputs of the Device.**

FIGURE 2. Terminal connections- continued

Truth Table 1/ 2/ 3/ 4/ 5/ 6/ 7/

Operation	K	$\overline{RPS}$	$\overline{WPS}$	DQ	DQ
Write Cycle: Load address on the rising edge of $\overline{K}$ clock; input write data on K and $\overline{K}$ rising edges.	L-H	X	L	D(A + 0) at K(t) ↑	D(A + 1) at $\overline{K}$ (t) ↑
Read Cycle: Load address on the rising edge of K clock; wait one and a half cycle; read data on $\overline{C}$ and C rising edges.	L-H	L	X	Q(A + 0) at $\overline{C}$(t +1) ↑	Q(A + 1) at C(t +2) ↑
NOP: No Operation	L-H	H	H	D = X Q = High Z	D = X Q = High Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

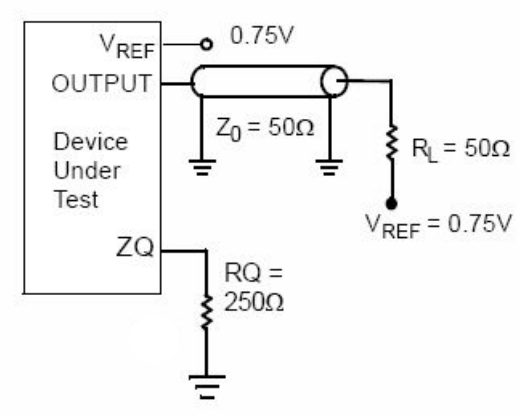
Write Cycle Descriptions 1/

$\overline{BWS_0}$/ $\overline{NWS_0}$	$\overline{BWS_1}$/ $\overline{NWS_1}$	K	$\overline{K}$	Comments
L	L	L-H	-	During the data portion of a write sequence both bytes ($D_{[17:0]}$) are written into the device.
L	L	-	L-H	During the data portion of a write sequence both bytes ($D_{[17:0]}$) are written into the device.
L	H	L-H	-	During the data portion of a write sequence only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9}$ remains unaltered.
L	H	-	L-H	During the data portion of a write sequence only the lower byte ($D_{[8:0]}$) is written into the device, $D_{[17:9}$ remains unaltered.
H	L	L-H	-	During the data portion of a write sequence only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0}$ remains unaltered.
H	L	-	L-H	During the data portion of a write sequence only the upper byte ($D_{[17:9]}$) is written into the device, $D_{[8:0}$ remains unaltered.
H	H	L-H	-	No data is written into the devices during this portion of a write operation.
H	H	-	L-H	No data is written into the devices during this portion of a write operation.

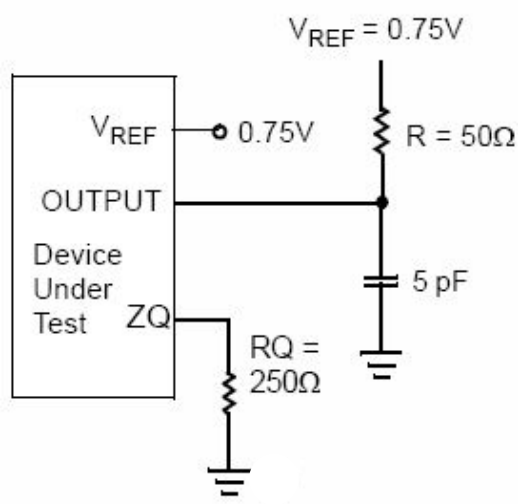
Notes

1. X= “Don’t Care,” H = Logic HIGH, L= Logic LOW, ↑ represents rising edge.
2. Device powers up deselected with the outputs in a tri-state condition.
3. “A” represents address location latched by the devices when transaction was initiated. A + 0, A + 1 represents the internal address sequence in the burst.
4. “t” represents the cycle at which a Read/Write operation is started. t + 1, and t + 2 are the first and second clock cycles respectively succeeding the “t’ clock cycle.
5. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
6. It is recommended that K = $\overline{K}$ and C = $\overline{C}$= HIGH when clocked is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
7. Is based on a write cycle that was initiated in accordance with the Write Cycle Descriptions table. $\overline{BWS_0}$ and $\overline{BWS_1}$ can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

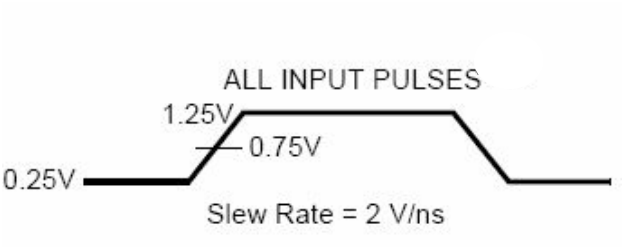
FIGURE 3. Truth table and device operations.



(a)



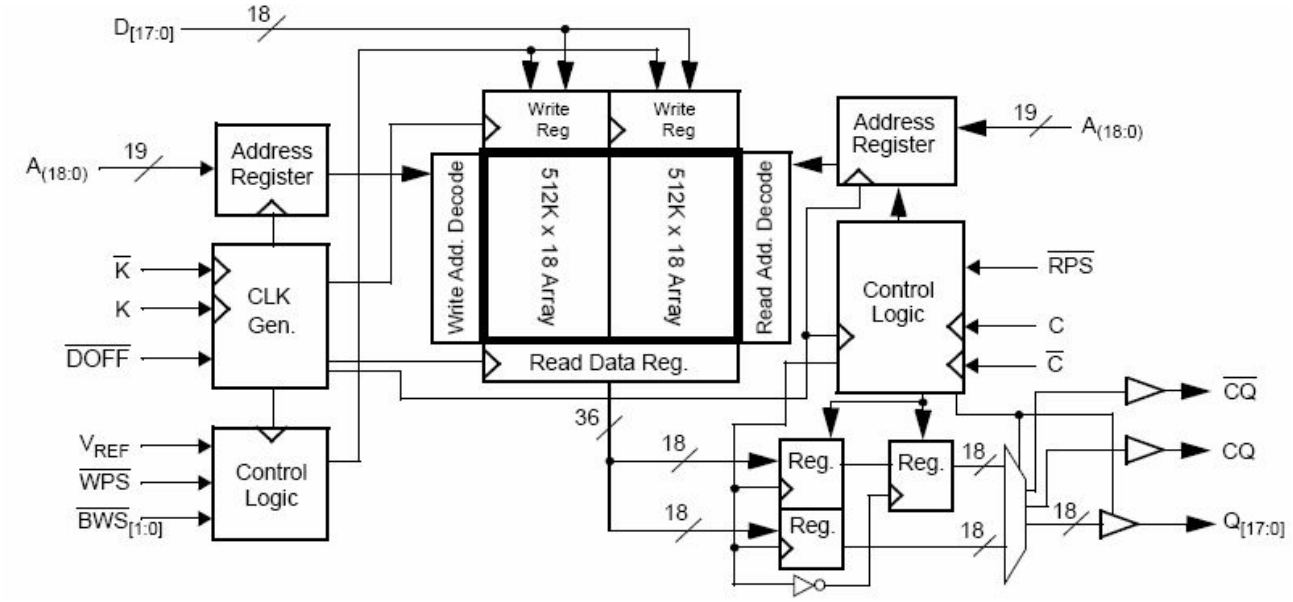
(b)



NOTES:
1. Use these output load circuits or equivalent for testing.
2. Capacitive load consists of all components of the test environment, including jig and scope.

FIGURE 4. Output load circuits.

BLOCK DIAGRAM



POWER UP WAVEFORMS

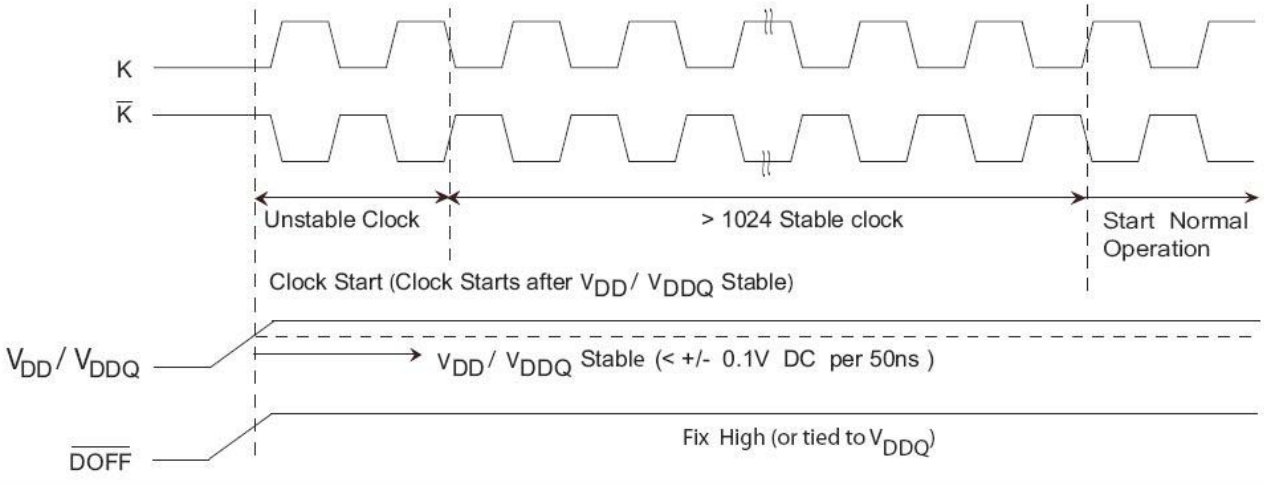
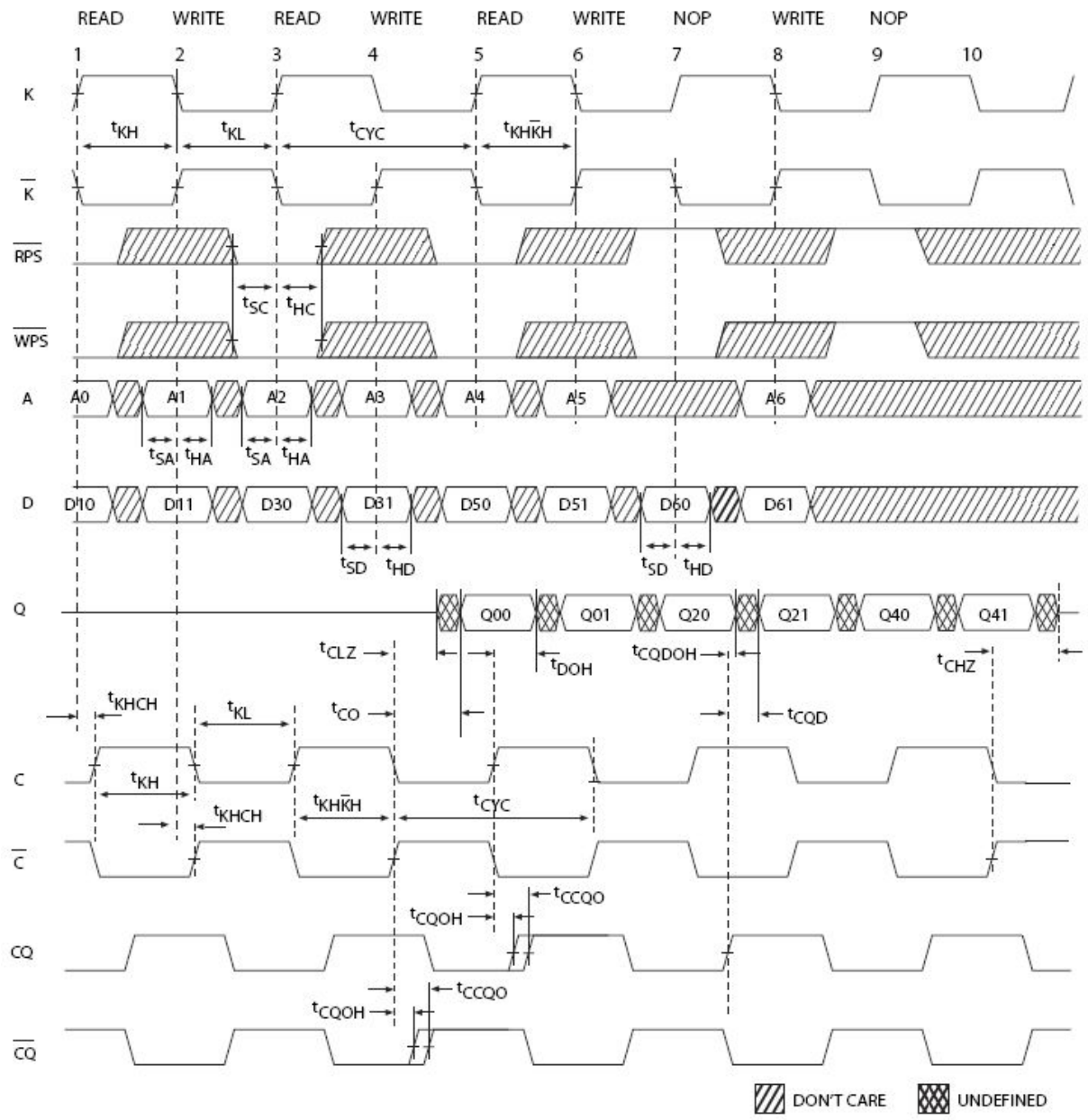


FIGURE 5. Timing waveforms.

READ/WRITE/DESELECT SEQUENCE 1/ 2/ 3/



1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, that is, A0 + 1.
2. Outputs are disabled (High Z) one clock cycle after a NOP.
3. In this example, if the address A0 = A1, then data Q00 = D10 and Q01 = D11. Write data is forwarded immediately as read results. This note applies to the whole diagram.

FIGURE 5. Timing waveforms - continued

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/

Line No.	Test Requirements	Subgroups (In accordance with MIL-PRF-38535, Table III)		
		Device Class N	Device Class Q	Device Class V
1	Interim electrical parameters (See 4.2)			1, 7, 9
2	Static Burn-In I Method 1015	Not Required	Not required	Required
3	Same as Line 1			1*, 7* Δ
4	Dynamic Burn-In (Method 1015)	Required	Required	Required
5	Same as Line 1			1*, 7* Δ
6	Final Electrical Parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A Test Requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7,8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7,8A, 8B, 9, 10, 11
8	Group C End-Point Electrical Parameters	2, 3, 7, 8A, 8B	2, 3,7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D End-Point Electrical Parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E End-Point Electrical Parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.
8/ Group A testing is not required if the requirements of MIL-PRF-38535 appendix B paragraph (B.4.2.a) have been accomplished.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	All device types
I_{SB1}	±10% of specified value in table I
I_{LK}, I_{OZ}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes N, Q and V. Qualification inspection for device classes N, Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein. Group A testing is not required if all tests have been performed during final electrical of the 100% Screening test. See footnote 8/ for table IIA.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes N, Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes N, Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes N, Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25ºC ±5ºC, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q and V.

5.2 Special Class N handling. Class N device is rated as a Moisture Sensitivity Level 3 part when tested per J-STD-020A. Device will be baked and dry packed when shipped from the manufacturer. Device will require a 125°C dry bake for 24 hours prior to installation if prolonged exposure on normal factory floor of the end user has occurred.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

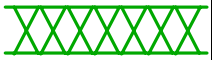
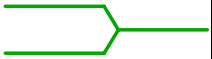
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the

system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-XX-XX

Approved sources of supply for SMD 5962-08SMD are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0823701NXA	6S055	DPA1312CV1825005A
5962-0823702NXA	6S055	DPA1312CV1820005A
5962-0823703NXA	6S055	DPA1312CV1816705A

1/ The lead finish shown for each PIN is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
6S055	DPA Components International 2251 Ward Avenue Simi Valley, CA 93065

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.