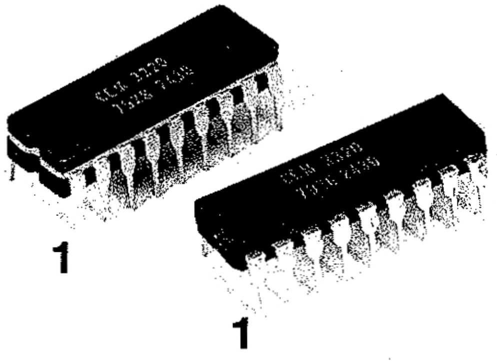
CURTIS ELECTROMUSIC SPECIALTIES

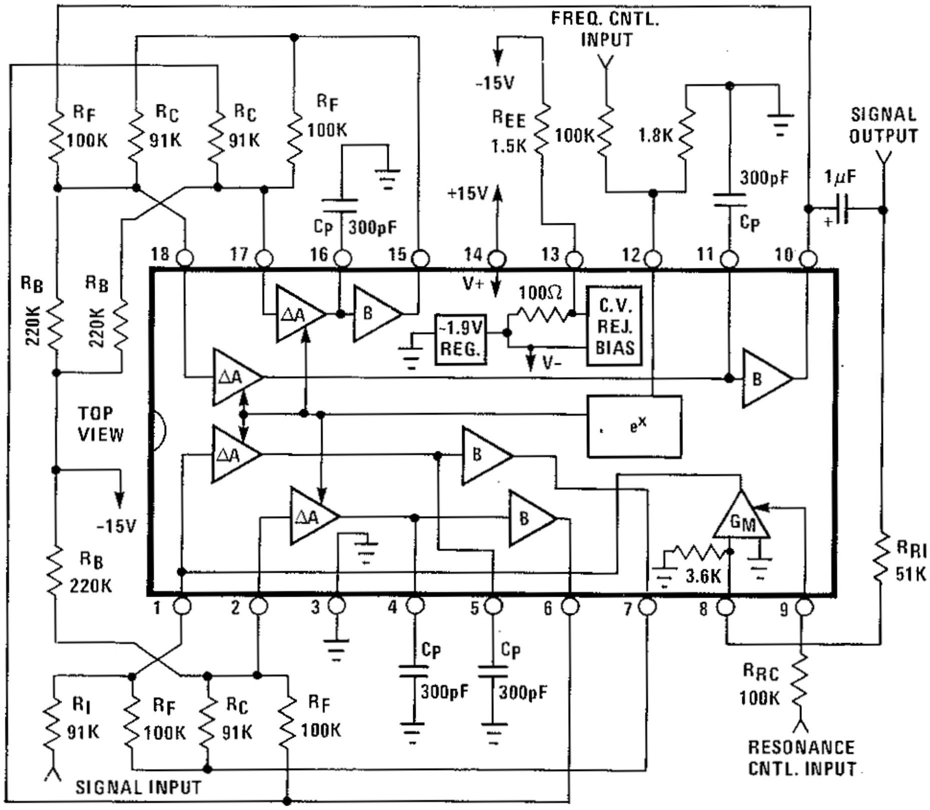
CEM 3320

Voltage Controlled Filter

The CEM 3320 is a high performance voltage controlled four-pole filter complete with on-chip voltage controllable resonance. The four independent sections may be interconnected to provide a wide variety of filter responses, such as low pass, high pass, band pass and all pass. A single input exponentially controls the frequency over greater than a ten octave range with little control voltage feedthrough. Another input controls the resonance in a modified linear manner from zero to low distortion oscillation. For those demanding applications, provision has been made to allow trimming for improved control voltage rejection. Each filter section features a novel variable gain cell which, unlike the traditional cell, is fully temperature compensated, exhibits a better signal-to-noise ratio and generates its low distortion predominantly in the second harmonic. The device further includes a minus two volt regulator to ensure low power dissipation and consequent low warm-up drift even with ±15 volt supplies.



Circuit Block and Connection Diagram



Features

- Low Cost
- Voltage Controllable Frequency: 12 octave range minimum
- Voltage Controllable Resonance: From zero to oscillation
- Accurate Exponential Frequency Scale
- Accurate Linear Resonance Scale
- Low Control Voltage Feedthrough: -45dB typical
- Filter Configurable into Low Pass, High Pass, All Pass, etc.
- Large Output: 12V.P.P. typical
- Low Noise: -86dB typical
- Low Distortion in Passband: 0.1% typical
- Low Warm Up Drift
- Configurable into Low Distortion Voltage Controlled Sine Wave Oscillator
- ±15 Volt Supplies

CEM 3320

Electrical Characteristics

$V_{CC} = +15V$ $R_F = 100K$ $T_A = 25°C$

Parameter	Min.	Typ.	Max.	Units
Pole Frequency Control Range	3500:1	10,000:1	–	
Sensitivity of Pole Frequency Control Scale, Midrange	57.5	60	62.5	mV/decade
Tempco of Pole Frequency Control Scale	3000	3300	3600	ppm
Exponential Error of Pole Frequency Control Scale[1]	–	4	12	%
Gain of Variable Gain Cell at V_C=0	0.7	0.9	1.3	
Max Gain of Variable Gain Cell	2.4	3.0	3.6	
Tempco of Variable Gain Cell[2]	–	500	1500	ppm
Output Impedance of Gain Cell[2]	0.5	1.0	2.0	MΩ
Pole Frequency Control Feedthrough	–	60	200	mV
Pole Frequency Warm-up Drift	–	.5	1.5	%
Gm of Resonance Control Element at I_{CR}=100uA	.8	1.0	1.2	mmhos
Amount of Resonance Obtainable Before Oscillation	20	30	–	dB
Resonance Control Feedthrough[3]	–	0.2	1.5	V
Output Swing At Clipping	10	12	14	V.P.P.
Output Noise re Max Output[4]	-76	-86	–	dB
Rejection in Bandreject	73	83	–	dB
Distortion in Passband[5,7]	–	0.1	0.3	%
Distortion in Bandreject[6,7]	–	0.3	1	%
Distortion of Sine Wave Oscillation[8]	–	0.5	1.5	%
Internal Reference Current, I_{REF}	45	63	85	μA
Input Bias Current of Frequency Control Input	0.2	0.5	1.5	μA
Input Impedance to Resonance Signal Input	2.7	3.6	4.5	KΩ
Buffer Slew Rate	1.5	3.0	–	V/uS
Buffer Input Bias Current (I_{EE}=8mA)	±8	±30	±100	nA
Buffer Sink Capability	.4	.5	.63	mA
Buffer Output Impedance[2]	75	100	200	Ω
Positive Supply Range	+9	–	+18	V
Negative Supply Range[9]	-4	–	-18	V
Positive Supply Current	3.8	5	6.5	mA

Note 1: $-25mV < V_C < +155mV$. Most of this error occurs in upper two octaves.

Note 2: $V_C = 0$

Note 3: Untrimmed. $0 < I_{CR} < 100\mu A$

Note 4: Filter is connected as low pass and set for 20 KHz cut-off frequency.

Note 5: Output signal is 3dB below clipping point.

Note 6: Output signal is 3dB below passband level, which is 3dB below clipping point. In general, this is worst case condition.

Note 7: Distortion is predominantly second harmonic.

Note 8: Sinewave is not clipped by first stage.

Note 9: Current limiting resistor always required.

Application Hints

Supplies

In order to minimize the power dissipation, the negative supply is regulated at -1.9 volts with an internal shunt regulator. This not only reduces warm-up drift of the pole frequencies at power turn-on, but also allows virtually any negative supply greater than -4 volts to be used. The current limiting resistor, R_{EE}, must always be included and is calculated as follows:

$$R_{EE} = \frac{V_{EE} - 2.7V}{0.008}$$

As can be seen from the Block Diagram, an internal 100Ω resistor is in series between the regulator and pin 13. This resistor, which allows for trimming of the control voltage feedthrough (explained in further detail below) results in an actual voltage at pin 13 of around -2.7 volts.

Although the circuit was designed for a positive supply of +15 volts, any voltage between +9 and +18 volts may be applied to pin 14. The only effect, other than power dissipation, is the maximum possible peak-to-peak output swing in accordance with:

$$V_{OUT}\ (V.P.P.) = V_{CC} - 3V$$

Operation of Each Filter Stage

Each filter stage consists of a variable gain cell followed by a high input impedance buffer. The variable gain cell is a current-in, current-out device (as opposed to the traditional voltage-in, current-out device) whose output current, I_{OUT}, is given by the following expression:

$$I_{OUT} = (I_{REF} - I_{IN}) A_{IO} e^{-V_C/V_T}$$

where $V_T = KT/q$, V_C is the

voltage applied to pin 12, A_{IO} is the current gain of the cell at $V_C = 0$ (Nominally 0.9), and

$$I_{REF} = \frac{.46V_{CC} - .65V}{100K^*}$$

*±25%

As the input to the variable cell is a forward biased diode to ground, it presents essentially a low impedance summing node at a nominal 650mV above ground. The required input currents may therefore be obtained with resistors terminating at this input node.

For normal operation of any filter type, each stage is set up with a feedback resistor, R_F, from the buffer output to the variable gain cell input, and with the pole capacitor, C_P, connected to the output of the variable gain cell. This setup is shown in Figure 1. In the D.C. quiescent state, the buffer output will always adjust itself so that a current equal to I_{REF} flows into the input.

For lowest control voltage feedthrough and maximum peak-to-peak output signal, the quiescent output voltage of each buffer, V_{ODC}, should be:

$$V_{ODC} = .46V_{CC}$$

Thus, in the simple case of Figure 1, R_F is calculated as follows:

$$R_F = \frac{V_{ODC} - .65V}{I_{REF}}$$

$$= 100K \text{ nominal}$$

Since I_{REF} can vary ±25%, V_{ODC} can vary nearly 30% from device to device using a standard 5% resistor for R_F. In the typical case where $V_{CC} = +15V$, I_{REF} is $63\mu A$ nominal, and the D.C. output of each buffer should be set for +6.9V nominal.

Absolute Maximum Ratings

Voltage Between V_{CC} and V_{EE} Pins	+22V,-0.5V
Voltage Between V_{CC} and Ground Pins	+18V,-0.5V
Voltage Between V_{EE} and Ground Pins	-4V,+0.5V
Voltage Between Cell Input and Ground Pins	+0.5V,-6V
Voltage Between Frequency Control and Ground Pins	±6V,
Voltage Between Resonance Control and Ground Pins	+2V,-18V
Current Through Any Pin	±40mA
Storage Temperature Range	-55° C to +150° C
Operating Temperature Range	-25° C to +75° C

The output impedance of the variable gain cell, although high, has a finite value. This impedance is reflected back to the input as an A.C. resistance of nominally 1 megohm in parallel with the feedback resistor, R_F, regardless of control voltage value. The pole frequency of each filter section is determined by the total equivalent feedback resistance, R_{EQ}, and the pole capacitor in the expression:

$$f_P = \frac{A_{IO}}{2\pi R_{EQ} C_P} e^{-V_C/V_T}$$

where:

$$R_{EQ} = \frac{R_F \cdot 1M\Omega^*}{R_F + 1\,M\Omega^*}$$

*-50%, +100%

Signal Coupling into a Filter Section

For the filter section to provide the low pass function, the input signal is coupled via a scaling resistor, R_C, into the input. If the signal is the external input to the entire filter, it will in general have a D.C. quiescent voltage level of zero, and all of I_{IN} equal to I_{REF} for the first stage will be provided by its feedback resistor. If the signal is from the output of a previous filter section, it will have a quiescent level of $.46V_{CC}$ (6.9 volts for a +15 volt supply). Therefore, part of I_{IN} will be supplied by this voltage through R_C while the remainder will be sourced through R_F.

The voltage gain in the passband is given by R_{EQ}/R_C. In general, this gain should be set to unity for stages two, three and four. The input resistor to stage one can be scaled for any size of the external input signal. The resistance value should be selected so that the maximum external input signal produces the maximum passband output signal before clipping.

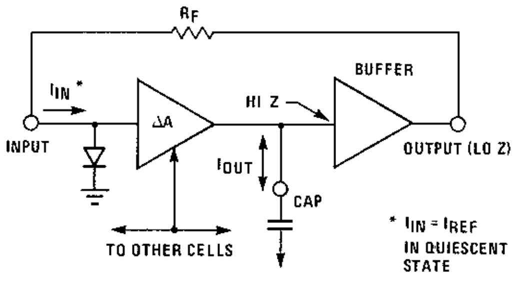


FIGURE 1: ONE OF FOUR STAGES

To generate the hi-pass function, the input signal is coupled into the variable gain element output via the pole capacitor, C_P. Therefore, any D.C. voltage level is blocked by the capacitor and I_{IN} equal to I_{REF} for each input is supplied only through the feedback resistors. The voltage gain in the pass band is simply unity, regardless of the value of R_F. For best results, the output impedance of whatever is generating the external input signal to stage one should be low compared to $R_F/4$.

Sample Filter Circuits

The Block Diagram shows the external components connections for a four-pole, low-pass filter designed to operate off ±15 volt supplies. The values for R_F, R_C, and R_B were chosen so that a) when the 1 megohm reflected resistance is in parallel with R_F, the gain of stages two, three and four is unity, and b) with the buffer outputs at the proper quiescent level of 6.9 volts, the total current into each input is the required $63\mu A$. For stage 1, all of this quiescent current is sourced by the feedback resistor. For stages two, three, and four, $63\mu A$ is sourced by the feedback resistor, while $70\mu A$ is sourced by the coupling resistor for a total sourced current of $133\mu A$. Thus, to end up with a net quiescent input current of $63\mu A$, $70\mu A$ is sunk out of the input by bias resistor, R_B.

If connecting the filter input to an external signal causes the D.C. level of the filter output to change more than several volts, it is recommended that an input coupling capacitor be used such as shown in Figure 4.

Figures 2, 3, 4, and 5 show high-pass, band-pass, all-pass, and state variable realizations, all with the voltage controlled resonance feature. Note that due to the configuration of the resonance feedback, the resonance frequency of the high-pass will be approximately 2.4 times higher than that of the low-pass, while the resonance frequency of the band-pass and all-pass will be 1/2.4 = .42 times lower than that of the low-pass, for the same component values. For the state variable, resistor R_Q adds positive feedback to increase the maximum Q, which is otherwise limited by the reflected 1MΩ impedance across the integrators.

Pole Frequency Control Scale

The current gains of each of the four sections (and consequently their pole frequencies) are controlled simultaneously with a voltage applied to pin 12. Since the scale is exponential with the standard 18mV/octave (60mV/decade), an input attenuator network will in most cases be required. An increasing positive control voltage lowers the pole frequencies of the filter. For best results over a thousand-to-one control range, the voltage on pin 12 should be maintained between -25mV and +155mV.

Unlike the typical variable transconductance cell used in most V.C. filters, the four stages in the CEM 3320 are fully temperature compensated. The only remaining first order temperature effect is that of control scale sensitivity $(1/V_T)$. This effect may be compensated in the usual manner with a +3300ppm tempco resistor (Tel Labs Q81).

Resonance Control

The variable gain cell used to control the amount of resonance is the traditional transconductance type of amplifier. It has a separate signal voltage input (pin 8), a separate control current input with a modified linear scale (pin 9), and a current output internally connected to the input of stage one. With an impedance of 3.6K ±900Ω, the input is referenced to ground; thus, connection to the filter output will require a coupling capacitor.

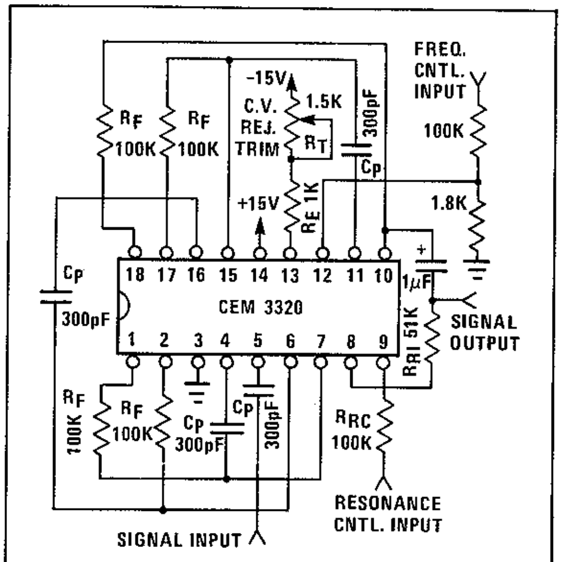


FIGURE 2: HI PASS FILTER WITH V.C. RESONANCE

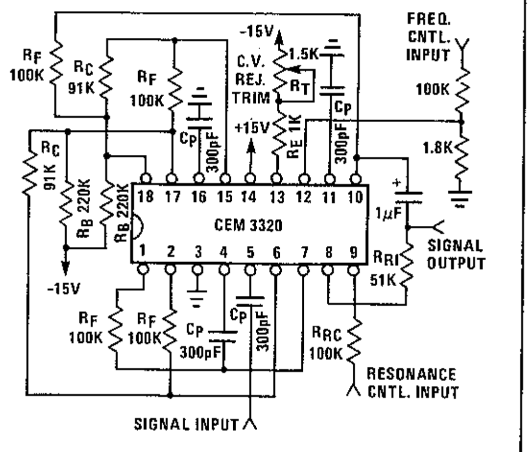


FIGURE 3: BAND PASS FILTER WITH V.C. RESONANCE

Control of the transconductance is accomplished with a current input. As the control input is a low impedance summing node at a potential near ground, the control current may be derived from the resonance control voltage with an input resistor, R_{RC}, terminated at pin 9. This resistor should be selected so that the maximum available resonance control voltage produces the maximum desired control current.

Figure 6 shows a graph of the transconductance versus control current. As can be seen, the slope of the curve becomes more gradual as the control current increases. This feature allows the resonance to be controlled with finer resolution as the critical point of oscillation is approached.

The maximum control current is therefore selected in accordance with the amount of control sensitivity which is desired at the top of the control range. The value of the input resistor, R_{RI}, is then selected depending on where in the control scale oscillation is desired to begin (when the control voltage is 90% of the maximum value, for instance). The following formula may be used:

$$R_{RI} = 3.6K^{*} \left(\frac{Gm_{OSC} R_{EQ} - 1}{A_{OSC}} \right)$$

*±25%

where Gm_{OSC} is the transconductance corresponding to the control current at which oscillation is desired to begin; and where A_{OSC} is the overall gain from the resonance signal input resistor, R_{RI}, to the filter output required to sustain oscillation. If the gain of stages 2, 3 and 4 are unity, then A_{OSC} = 12dB or 4 in the case of the low pass filter.

While operating the filter in the resonant mode, care should be taken not to overload the input to the filter. If the signal output of stage one is allowed to become clipped, then not only will the apparent resonance of the signal at the filter output appear to be reduced, but the D.C. level of the output signal will shift.

When the resonance control is advanced until sustained oscillations are produced, advancing the resonance control further will merely increase the amplitude of the oscillation. A lesser effect is the shift of the oscillation frequency. For minimum shift (typically less than 0.5%), the oscillation amplitude should be kept below the clipping level of the first stage output. Allowing the oscillation to be clipped will produce frequency shifts in excess of 5%.

Other Uses of the Resonance Control Cell

Other than controlling the resonance, the variable transconductance amplifier may be used as an independent VCA controlling the amplitude of the input signal to the filter. Or the cell may be set up as a symmetrical limiter/clipper for either preventing large dynamic input signals from overloading the filter or for providing additional coloration to the input signal.

Pole Frequency Control Voltage Rejection

The D.C. voltage shift at the filter output due to the frequency control voltage may be minimized by adjusting the current into the minus supply pin, pin 13. This is accomplished by replacing the negative supply current limiting resistor, R_{EE}, with a series resistor and trim pot. The fixed resistor, R_E, and series trim pot, R_T, should be selected so that the current into pin 13 may be adjusted from 5mA to 12mA. Or:

$$R_E = \frac{V_{EE} - 3.2V}{12mA}$$

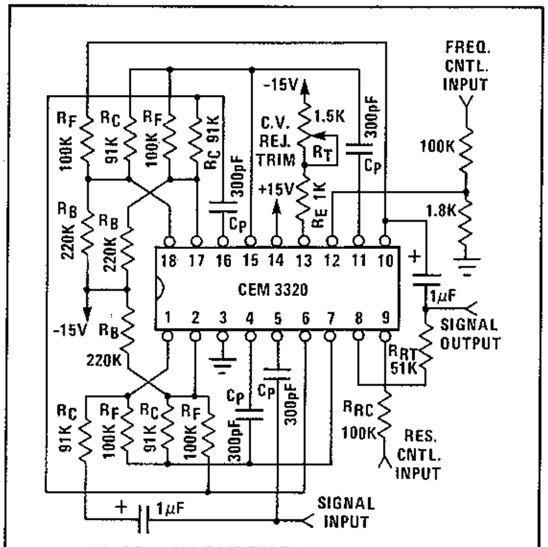


FIGURE 4: ALL PASS FILTER WITH V.C. RESONANCE

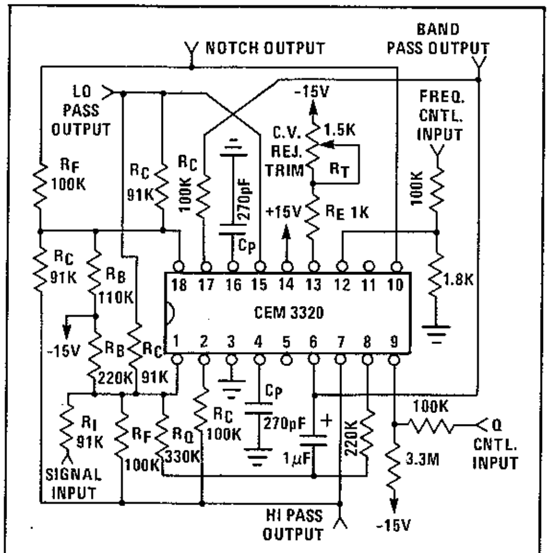


FIGURE 5: STATE VARIABLE FILTER WITH V.C. "Q"

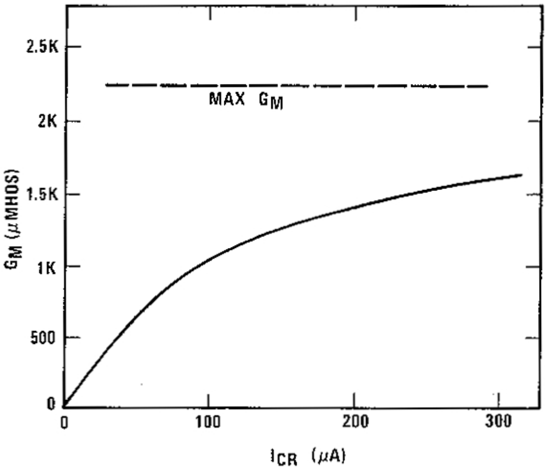


FIGURE 6: TRANSCONDUCTANCE V.S. CONTROL CURRENT OF RESONANCE CELL

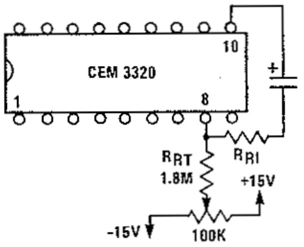


FIGURE 7: TRIMMING OF RESONANCE C.V. FEEDTHROUGH

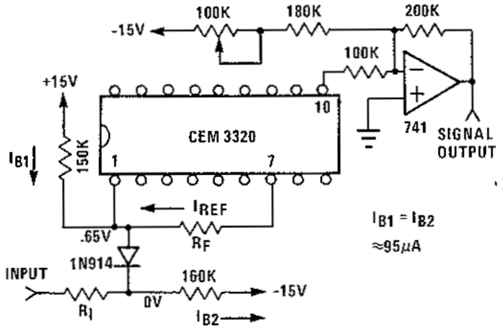


FIGURE 8: ZERO REFERENCING THE INPUT AND OUTPUT

and

$$R_T = \frac{V_{EE} - 2.4V}{5mA} - R_E$$

These components are shown in the filter circuits of Figures 2–5. To obtain minimum control voltage feedthrough, the best technique for adjusting this trim is to switch back and forth between the maximum and minimum control voltages while adjusting the pot so that the D.C. output voltage at these two extreme conditions is the same.

Resonance Control Voltage Rejection

For most applications, no trimming should be necessary. However, if required, the resonance control voltage feedthrough may be minimized by applying a small D.C. voltage on the resonance signal input pin, pin 8. A typical set-up is shown in Figure 7. The value of R_{RT} should be selected so the trim pot is able to adjust the voltage on pin 8 by ± 30mV.

Stage Buffers

Each buffer can source up to 10mA and sink a nominal 500μA. However, any D.C. load greater than ±200μA to ±300μA may begin to degrade the performance of the filter, especially if the loads on each buffer differ by more than this amount. The maximum recommended D.C. loads are 1mA source, 250μA sink, and a 150μA load difference between buffers. The maximum recommended A.C. loads are ±250μA.

Since the D.C. level at the filter output is at some non-zero voltage (6.9 volts for V_{CC} = +15V), a coupling capacitor will be required somewhere in the signal chain, either at the filter output or the following device inputs. Note that if the resonance feature is being used, the filter output is already D.C. blocked by the resonance input coupling capacitor, thus providing a convenient output point. If D.C. coupling to ground referenced inputs and outputs is required, the schemes shown in Figure 8 may be used. Note that the output circuit has the benefits of 1) allowing for gain after the filter, and 2) providing an output with greater drive capability. The buffer outputs are not short circuit protected; therefore care should be exercised to not short the outputs to ground or either supply.